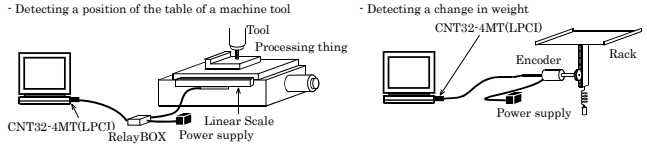
4ch 32Bit High-Speed Up/Down Counter Board for Low Profile PCI (TTL Input)

CNT32-4MT(LPCI)

* Specifications, color and design of the products are subject to change without notice.

This is a PCI bus compliant interface board for counting the pulses input from the external device.
The board supports a low-profile PCI slot and, if replaced with the supplied bracket, supports a PCI slot, too.
The board has four channels of 32-bit up/down counters, allowing external devices such as a rotary encoder and a linear scale to be connected. Given below are examples of using the board for “detecting a position of the table of a machine tool” and “detecting a change in weight”.
The pulse signal inputting interface is unisolated LVTTL-level input that can input pulse signals at high speed.
The application for this board can transfer data between the board and the PC at high speed using PCI bus mastering.

<Example >



Features

Can input two-phase and single-phase signals.

Can input pulse signals up to 10MHz and can resolve phase differences as short as 25nsec.

Can be converted to a differential input interface using the differential unit (CTP-4D) and connection cable (CNT-68M/50M) which are sold separately.

One control signal input pin per channel.

Can count values sampling at a maximum sampling rate of 20 MHz.

Supporting bus mastering, enabling high-speed data transfer between the board and the PC without intervention from the CPU.

Can generate an interrupt, issuing an external signal, or presetting/zero-clearing the count value when it matches an arbitrary predefined value.

Support for both of low-profile and standard PCI slots (interchangeable with a bundled bracket).

Specification

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Item			Specification
Input			
	Counter		
		Channel count	4 channels
		Count system	Up/down counting (2-phase/Single-phase/Single-phase Input with Gate Control Attached)
		Max. count	FFFFFFFFh(binary data, 32Bit)
		Input type	Unisolated LVTTL level input
		Input signal	Phase-A/UP 1 x 4 channels Phase-B/DOWN 1 x 4 channels Phase-Z/CLR 1 x 4 channels
		Response frequency	10MHz 50% duty
		Digital filter	0.1µsec - 1.6384msec or not used (can be independently set for each channel.)
		Timer	1msec - 6553msec 1msec unit
		Counter start trigger	Software/External start input/Sampling start trigger
		Counter stop trigger	Software/External stop input/Sampling stop trigger
	Sampling		
		Sampling start trigger	Software/External start input/Count match
		Sampling stop trigger	Software/External stop input/Specification number/Bus master tranfer error/Count match
		Sampling clock	Sampling timer/External clock input
		Sampling timer	50nsec - 107sec 25nsec unit(can not be independently set for each channel.)
		External sampling start signal	Unisolated LVTTL level input (Select Rise or Fall)
		External sampling stop signal	Unisolated LVTTL level input (Select Rise or Fall)
		External sampling clock signal	Unisolated LVTTL level input (Fall)
		Response frequency	10MHz 50% duty
	Control		
		Control input signal type	Unisolated LVTTL level input
		Control input channel	1 x 4 channels
		Control input signal	- Preset(Select Rise or Fall) - Zero-clear(Select Rise or Fall) - Counter start/stop(Select Rise or Fall) - General-purpose input(positive logic) Software-selected from among the above four options
		Response time	100nsec (Max.)
	Interrupt event		Count match(8 points), Counter error(2 points), Sampling factor(6 points), Carry/Borrow(1 points), Timer(1 points)

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Item			Specification
Output			
	Control		
		Control output signal type	Unisolated LVTTL level output
		Control output channel	1 x 4 channels
		Control output signal	- Count match 0 output(one-shot pulse output) - Count match 1 output(one-shot pulse output) - Digital filter error output(one-shot pulse output) - Abnormal input error output(one-shot pulse output) - General-purpose output(Level output) Software-selected from among the above five options (Positive/negative logic is selected with the software.)
		One shot output signal amplitude	Selected between 10μsec, 100μsec, 1msec, 10msec and 100 msec (Can be set for each channel, within precision + 1μsec)
		Response time	100nsec (Max.)
		Rated output current	I_{OL}=8mA(Max.) I_{OH}=-8mA(Max.)
	Test pulse		
		Test pulse output signal type	Unisolated LVTTL level output
		Test pulse output point	One for each of phases-A and B
		Output frequency	100kHz fixed
	Sampling		
		Sampling output signal type	Unisolated LVTTL level output
		Output point	Sampling start trigger, sampling stop trigger, Sampling clock trigger 1 point each
		One-shot output signal width	Negative logic 100nsec (fixed)
		Response speed	100nsec (Max.)
		Rated output current	I_{OL} = 8mA(Max.) I_{OH} = -8mA(Max.)
Bus master			
	DMA channel		1 channel
	Transfer bus width		32-Bit width
	Transfer data length		8 PCI Words length(Max.)
	Transfer rate		80MB/sec(Max.133MB/sec)
	FIFO		1K-DWord
	Scatter/Gather function		64MB
	Interrupt event		Bus master event(7 points)
Common			
	I/O address		Occupies 2 locations, any 32-bytets and 64-byte boundary
	Power consumption		5VDC 300mA (Max.)
	Operating condition		0 - 50°C, 10 - 90%RH (No condensation)
	PCI bus specification		33bit, 33MHz, Universal key shapes supported *1
	Dimension (mm)		121.69(L) x 63.41 (H)
	Weight		60g

*1 This board requires power supply at +5 V from an expansion slot (it does not work on a machine with a +3.3-V power supply alone).

Support Software

Driver Library API-PAC(W32) (Bundled)

API-PAC(W32) is the library software that provides the commands for CONTEC hardware products in the form of Windows standard Win32 API functions (DLL). It makes it easy to create high-speed application software taking advantage of the CONTEC hardware using various programming languages that support Win32 API functions, such as Visual Basic and Visual C/C++.
It can also be used by the installed diagnosis program to check hardware operations.
CONTEC provides download services to supply the updated drivers and differential files.
For details, read Help on the bundled CD-ROM or visit the CONTEC's Web site.

< Operating environment >

OS	Windows XP, 2000, Me, 98, etc..
Adaptation language	Visual C/C++, Visual Basic, Delphi, Builder, etc..
Others	Each piece of library software requires 50 MB of free hard disk space.

Cable & Connector

Cable(Option)

Shielded cable for CardBus counter input card
: CNT-68M/50M (0.5m)

Cable with 68-Pin D-sub Connector at either Ends (Mold Type)
: PCB68PS-0.5P (0.5m)
: PCB68PS-1.5P (1.5m)

Shielded cable with single connector for 68-pin 0.8mm pitch connector
: PCA68PS-0.5P (0.5m)
: PCA68PS-1.5P (1.5m)

Accessories

Accessories (Option)

Termination Panel with Differential Receivers for Counter Input : CTP-4D *1
Screw Terminal (M3 x 50P) : EPD-50A *1
Screw Terminal (M3 x 68) : EPD-68A *2

*1 CNT-68M/50M optional cable is required separately.
*2 PCB68PS-0.5P or PCB68PS-1.5P optional cable is required separately.

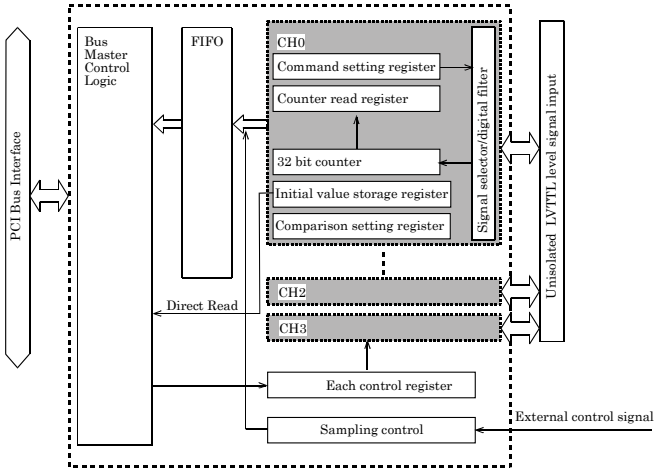
* Check the CONTEC's Web site for more information on these options.

Packing List

Board [CNT32-4MT(LPCI)] …1
First step guide … 1
CD-ROM *1 [API-PAC(W32)] …1
Bracket for PCI…1

*1 The CD-ROM contains the driver software and User's Guide.

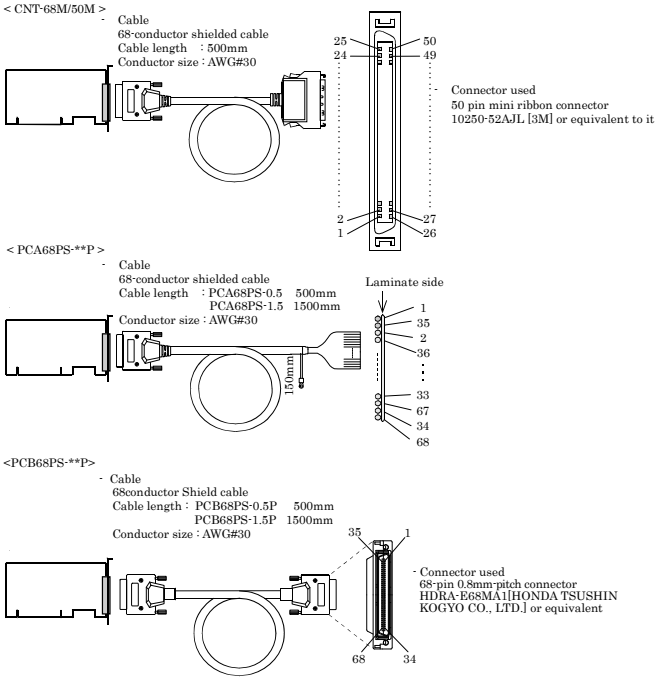
Block Diagram



Using the On- Board Connectors

Connecting a Board to a Connector

Use the optional connection cable (CNT-68M/50M or PCA68PS-**P, PCB68PS-**P) to connect the board to an external device. Uses the cable together with a terminal block for the wiring between the board and external device.



Connector Pin Assignment

Pin Assignment of an interface connector(CN1)(Board side)

CH0 phase-A input	A0	1	35	GND	Ground
CH0 Phase-B input	B0	2	36	GND	Ground
CH0 Phase-Z input	Z0	3	37	GND	Ground
CH0 control input *1	DI0	4	38	GND	Ground
Unconnection	N.C.	5	39	N.C.	Unconnection
CH1 Phase-A input	A1	6	40	GND	Ground
CH1 Phase-B input	B1	7	41	GND	Ground
CH1 Phase-Z input	Z1	8	42	GND	Ground
CH1 control input *1	DI1	9	43	GND	Ground
Unconnection	N.C.	10	44	N.C.	Unconnection
CH2 Phase-A input	A2	11	45	GND	Ground
CH2 Phase-B input	B2	12	46	GND	Ground
CH2 Phase-Z input	Z2	13	47	GND	Ground
CH2 control input *1	DI2	14	48	GND	Ground
Unconnection	N.C.	15	49	N.C.	Unconnection
CH3 Phase-A input	A3	16	50	GND	Ground
CH3 Phase-B input	B3	17	51	GND	Ground
CH3 Phase-Z input	Z3	18	52	GND	Ground
CH3 control input *1	DI3	19	53	GND	Ground
Unconnection	N.C.	20	54	N.C.	Unconnection
Sampling clock input	CLKIN	21	55	GND	Ground
Sampling stop input	STOPIN	22	56	STARTIN	Sampling start input
Unconnection	N.C.	23	57	N.C.	Unconnection
Sampling clock output	CLKOUT	24	58	GND	Ground
Sampling stop output	STOPOUT	25	59	STARTOUT	Sampling start output
Unconnection	N.C.	26	60	N.C.	Unconnection
Test pulse Phase-A output	TPOA	27	61	TPOB	Test pulse Phase-B output
Unconnection	N.C.	28	62	N.C.	Unconnection
CH0 control output *2	DO0	29	63	DO1	CH1 control output *2
CH2 control output *2	DO2	30	64	DO3	CH3 control output *2
Unconnection	N.C.	31	65	N.C.	Unconnection
Counter input signal pull up	PUP1	32	66	PUP2	Control input signal pull up
Unconnection	N.C.	33	67	N.C.	Unconnection
+3.3V output *3	Vcc	34	68	Vcc	+3.3V output *3

*1 The control input can serve as the general-input, counter start/stop, preset, and zero-clear.
*2 The control output can serve as the general-output, count match, abnormal input error and digital filter error.
*3 Supply-capable current is 500mA (Max.).

Pin Assignment of CNT-68M/50M

+3.3V Output *3	N.C.	25	50	Vcc	+3.3V Output *3
Counter Input signal pull-up	AGND	24	49	PUP2	Counter Input signal pull-up
CH2 control output *2	N.C.	23	48	DO3	CH3 control output *2
CH0 control output *2	AGND	22	47	DO1	CH1 control output *2
Test pulse Phase-A output	AI 04	21	46	TPOB	Test pulse Phase-B output
Sampling Stop Output	N.C.	20	45	STARTOUT	Sampling Start Output
Sampling Clock Output	AI 05	19	44	GND	Ground
Sampling Stop Input	N.C.	18	43	STARTIN	Sampling Start Input
Sampling Clock Input	AGND	17	42	GND	Ground
CH3 Control Input *1	AGND	16	41	GND	Ground
CH3 Phase-Z input	AI 06	15	40	GND	Ground
CH3 Phase-B input	N.C.	14	39	GND	Ground
CH3 Phase-A input	AI 07	13	38	GND	Ground
CH2 Control Input *1	N.C.	12	37	GND	Ground
CH2 Phase-Z input	AO START	11	36	GND	Ground
CH2 Phase-B input	AO STOP	10	35	GND	Ground
CH2 Phase-A input	AO EXCLK	9	34	GND	Ground
CH1 Control Input *1	DGND	8	33	GND	Ground
CH1 Phase-Z input	DO 00	7	32	GND	Ground
CH1 Phase-B input	DO 01	6	31	GND	Ground
CH1 Phase-A input	DO 02	5	30	GND	Ground
CH0 Control Input *1	DO 03	4	29	GND	Ground
CH0 Phase-Z input	DGND	3	28	GND	Ground
CH0 Phase-B input	CNT UPCLK	2	27	GND	Ground
CH0 Phase-A input	Reseved	1	26	GND	Ground

*1 The control input can serve as the general-input, counter start/stop, preset, and zero-clear.
*2 The control output can serve as the general-output, count match, abnormal input error and digital filter error.
*3 Supply-capable current is 500mA (Max.).

How to Connect the Counter Input Signal

You can connect to a rotary encoder or linear scale with a TTL level output circuit, or to an open-collector output circuit. The signal must be an LVTTL level input and can be up to 10MHz.
As pull-up resisters are provided on the board, connect the pull-up voltage (3.3V to 5.5V max.) to the pull-up pins if connecting to an open collector output circuit/TTL-level output circuit. (If using 3.3V, connect to the VCC pin on the board.) Not connecting the pull-up voltage may affect the counter input channel left unconnected.
For a two-phase input, connect both phase A and phase B. For a single phase input, connect to either phase A or phase B. If not using the Z phase, this does not need to be connected.

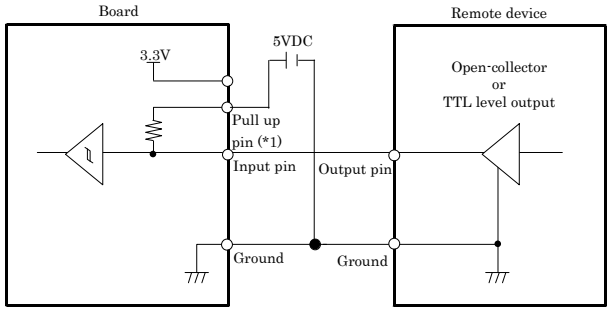
Remarks

The pull-up pins are PUP1 (pin 32 *1) for the counter input signal and PUP2 (pin 66 *1) for the control input signal.
PUP1 (pin 32):
Pull-up for A, B, and Z phase input signal
(A0, B0, Z0, A1, B1, Z1, A2, B2, Z2, A3, B3, Z3).
PUP2 (pin 66):
Pull-up for the control input signals and for the sampling input signals
(DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN).

*1 Connector pin number on the board.

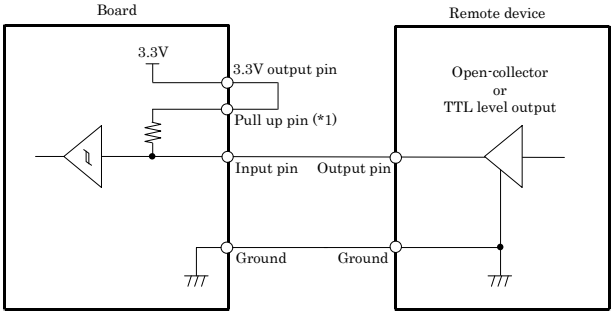
Example Connection for Counter Input Circuit

Connection pulled up with external 5-V power (Counter Input)



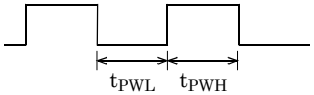
*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Connection pulled up with internal 3.3-V output power (Counter Input)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Input signal



t_{PWH} : High-level count input pulse width 50nsec (Min.)
t_{PWL} : Low-level count input pulse width 50nsec (Min.)

⚠ CAUTION

The connection cable length should be within 1.5 m.

To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.

Connecting the control signal input/ output

Connection of a control input

The control input signals consist of one pin per channel that can be selected as the channel's counter start/stop or preset, and one pin per board that can be used as the start, stop, and clock for sampling. The signals are LVTTL-level inputs.
As pull-up resisters (10KΩ) are provided on the board, connect the pull-up voltage (3.0V to 5.5V max.) to the pull-up pins if connecting to an open collector output circuit/TTL-level output circuit. (If using 3.3V, connect to the VCC pin on the board.) Not connecting the pull-up voltage may affect the control input pin left unconnected.

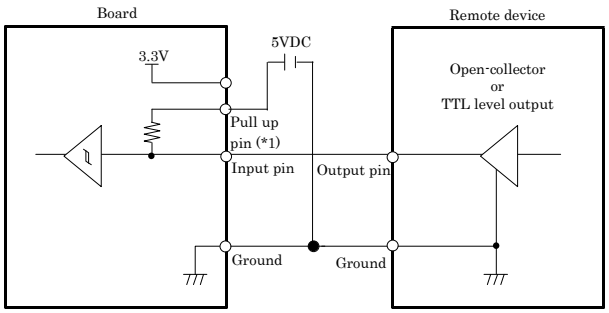
Remarks

The pull-up pins are PUP1 (pin 32 *1) for the counter input signal and PUP2 (pin 66 *1) for the control input signal.
PUP1 (pin 32):
Pull-up for A, B, and Z phase input signal (A0, B0, Z0, A1, B1, Z1, A2, B2, Z2, A3, B3, Z3).
PUP2 (pin 66):
Pull-up for the control input signals and for the sampling input signals (DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN).

*1 Connector pin number on the board.

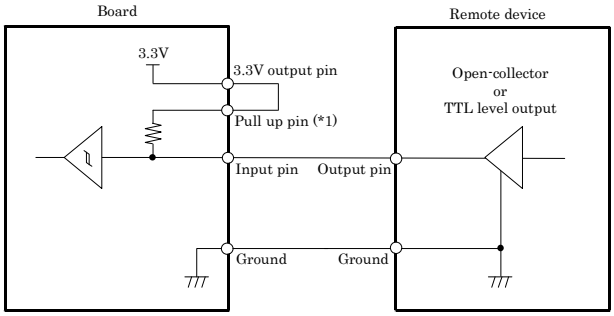
Control input circuit and its sample connection

Connection pulled up with external 5-V power (Control input DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

Connection pulled up with internal 3.3-V output power (Control input DI0, DI1, DI2, DI3, CLKIN, STARTIN, STOPIN)



*1: The pull-up pins are PUP1 for the counter input signal and PUP2 for the control input signal.

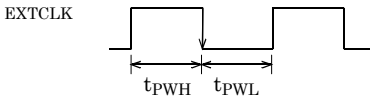
⚠ CAUTION

The connection cable length should be within 1.5 m.

To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.

External sampling clock signal (EXTCLK)

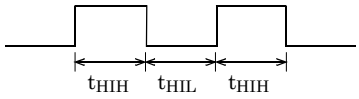
Pin used to input the external pacer clock. The maximum frequency is 10MHz.
If the external clock input is selected as the sampling clock, sampling occurs on the falling edge of the signal.



t_{PWH} : High-level clock pulse width 50nsec (Min.)
t_{PWL} : Low-level clock pulse width 50nsec (Min.)

Other control input signals (DI0 to DI3, EXTSTART, EXTSTOP)

These signals are TTL-level compatible and the trigger edge is software-programmable at either the rising or falling edge. High- and low-level hold times of at least 50 nsec are required to detect an edge of the signal.



t_{HIH} : High-level hold time 50nsec (Min.)
t_{HIL} : Low-level hold time 50nsec (Min.)

Connection of a control output

This outputs a general-purpose output signal (level output) or a one-shot pulse output to indicate a hardware event such as a count match. The signal is an LVTTL level output and can be set to positive or negative logic by software.

Control output circuit and its sample connection