PS5610/11 High Brightness LED Driver

Key Features

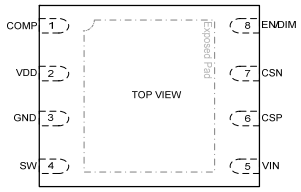
- Up to 95% Efficiency
- Wide Input Voltage Range: 4.75-55V
- 2A (max) Output Current
- Monolithic solution with Power FET
- Built-in PWM controlled DC/DC Converter
- Digital PWM control of LED Dimming
- Analog dimming option controlled by DC input (0.7 to 2.84V)
- Low DIM-off to SW rising edge delay (1µs)
- Fast LED current rise time
- Supports buck, boost, and buck-boost configurations
- Low-power sleep mode
- Over voltage protection, over current protection, thermal shutdown, and soft start

Applications

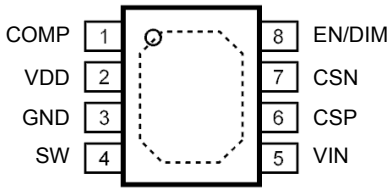
- General Illumination
- Architectural Lighting
- Streetlights / Park Lighting / Arena Lighting
- Special Illumination (Projectors, Spotlighting, Security, etc.)
- Appliance Lighting
- RGB LED Lighting Solutions

Main Specifications

• Supply Voltage	55V (max)
• Oscillator Frequency	1MHz (typical)
• LED Current	2A (max)
• Rds on Resistance (VIN >= 8V)	215mΩ typical
• Current Sense Voltage	100mV ±3%



MLPD 5mm x 6mm (Exposed Heat Slug)

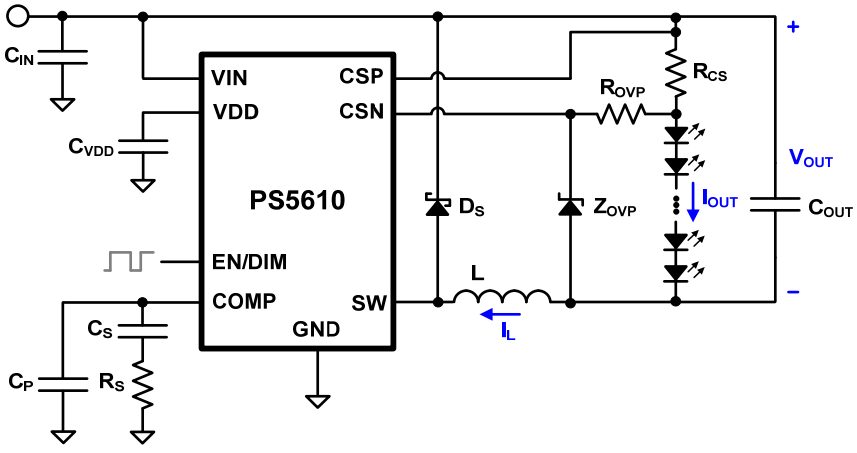


HSOP-8 (Exposed Heat Slug)

Overview

The PS5610 and PS5611 are wide input voltage range, high efficiency LED driver ICs, using current-mode PWM control. The ICs feature built-in power transistors and drive high-brightness LEDs with few external components. These ICs utilize a DC-DC converter architecture operating in CCM (continuous conduction mode) with a 1MHz switching frequency. The ICs deliver up to 2A of LED current. An external resistor sets the constant LED current, and the LED dimming can be controlled by either an analog or digital input. The advanced architecture is highly efficient in Buck, Boost, and Buck-Boost topologies.

Typical (Buck Mode) Implementation



Note: R_{OVP} and Z_{OVP} are optional devices that implement over voltage protection

1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	VIN_max	-0.3 to +60	V
Supply Voltage Slew Rate	dVin/dt	+1.0	V/µs
SW Voltage	VSW_max	-0.3 to +60	V
Current Sense Voltage	CSP_max, CSN_max	-0.3 to +60	V
Current Sense Differential Voltage	CSP-CSN	-0.3 to +0.3	V
All Other Pins		-0.3 to (5.5 or VIN+0.3, whichever is less)	V
Operating Junction Temperature	Tj	125	°C
Storage Temperature	Tstg	-40 to 150	°C
Human Body Model ESD Voltage	HBM	±2000	V
Machine Model ESD Voltage	MM	±200	V
Charge Device ESD Model	CDM	±2000	V

Note: Exceeding the values listed under Absolute Maximum Ratings may cause permanent damage to the device. Operating the device at or near the limits listed under Absolute Maximum Ratings for extended periods of time may affect device reliability.

2 Package Thermal Information (Static Environment, No Active Cooling)

Parameter	Symbol	Typical Rating	Units
Package Thermal Resistance, heat slug soldered to PCB(1)	Theta JA	25 (1,2)	°C/W
Package Thermal Resistance, heat slug not soldered to PCB(3)	Theta JA	95 (2)	°C/W
Maximum Reflow Temperature		260	°C
Maximum Reflow Time		20	s

(1) See JEDEC JESD51-5 and JESD51-7 for board configuration.

(2) Actual values will be application dependent.

(3) It is not recommended to run without the heat slug attached to the PCB at high power levels.

3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Ambient Operating Temperature	Ta	-40		85	°C
Supply Voltage	VIN	4.75		55	V
Positive Current Sense Common Mode Range	VCSP	4.75		55	V
EN/DIM Input		0		5	V
5V Linear Regulator Minimum VIN Voltage for VDD in spec	VDD_minVIN		7.4	8.2	V
5V Linear Regulator Maximum Output Current	Ivdd_max			5	mA
LED Current	Iout	0.02		2	A
Pk-Pk Inductor Ripple Current	ΔIL/IL			0.4	A/A
PWM Signal Frequency Range with Digital Input	m_a	1.3			A/µs
PWM Signal Frequency Range with Digital Input	Fpwm	35		10,000	Hz
Minimum PWM On Pulse Width	Tpwm_minOn	10			µs
Minimum PWM Off Pulse Width	Tpwm_minOff	10			µs
Maximum PWM Off Time	Tpwm_maxOff			29	ms
Maximum Dimming Ratio with Analog Input (Internal PWM)	DimRatioA		128:1		A/A
Maximum Dimming Ratio with Digital Input	DimRatioD	10:1		3200:1	A/A

Note: The device is not guaranteed to function outside of its recommended operating conditions.

4 Electrical Characteristics

VIN = 4.75V to 55V, TA = 25ºC (unless otherwise noted); specification values subject to change

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current, Sleep Mode	IQoff	VEN = 0V, t > EN_timer		17	40	µA
Supply Current, Output Disabled Mode	IQ2	VIN = 12V, VEN=0V, VCS = 0V, t < EN_timer		0.6	0.8	mA
Supply Current, Output Enabled Mode	IQ3	No external components connected to SW pin, VIN = 12V, VEN = 5V, VCS = 0V		5.0	6.0	mA
Current Sense Voltage (CSP - CSN)	VCS	Iout = 10mA to 2A Rcs = 100mV / Iout	97	100	103	mV
Current Sense Voltage Temperature Coefficient	VCS_tc	Tj = -40ºC to +125ºC		±10		µV/ºC
CSP input current	ICSP	Current into CSP pin		140	300	µA
CSN input current	ICSN	Current into CSN pin		0.16	2	µA
Error Amplifier Voltage Gain	AEA		60			dB
Error Amplifier Transconductance	GEA	ΔICOMP = ±10µA	4.15	5.2	6.25	mA/V
COMP to Current Sense Transconductance	GCS		3.3	5.4	7.1	A/V
Low Side Switch On Resistance, Package	Rds_on_LS	VIN = 4.75V to 8V, Iout = 1A		240		mΩ
		VIN = 8V to 55V, Iout = 1A		215	260	
High Side Switch On Resistance, Package	Rds_on_HS	R_{DS} = Δ(VSW)/Δ(ISW) for ISW = 10mA		70		Ω
Low Side Switch Leakage Current	I_leak	VEN = 0V, VSW = 2V			10	µA
Peak Current Limit	IS1	Vout = 5V to 10mV	2.6		4.4	A
Average Current Limit	IS2	Vout = 5V to 10mV	2.0			A
Soft Start Peak Current Limit	ISS	CSP – CSN < VSS After Sleep Mode	0.8			A
Line Regulation	Line_reg	Vin = 12V to 55V, Iout = 1A, Vout = 7.5V		<1	2	%

Parameter	Symbol	Condition	Min	Typ	Max	Units
Load Regulation	Load_reg	Vin = 55V, Iout = 1A Vout = 10V to 55V			6	%
Minimum On Time	Ton_min			100	120	ns
Maximum Duty Cycle	Dmax		92	95		%
Oscillator Frequency	Fosc		0.95	1.00	1.05	MHz
Internal PWM DIM Oscillating Frequency	Framp		924	977	1030	Hz
Internal PWM DIM Step Size	DIMA_step	Analog DIM step size	15.2	16.8	18.4	mV
DIM to SW Falling Edge Delay	TD			1.2	1.4	µs
Current Sense Over Voltage Protection, Rising Threshold	VCS_OVP	CSP – CSN	205		225	mV
Current Sense Soft Start Rising Threshold	VCS_SS	CSP – CSN After Sleep Mode	4	19	22	mV
Analog DIM Voltage for LED Guaranteed Off	VDIMAL	EN/DIM Terminal			0.64	V
Analog DIM Voltage for LED 100% Guaranteed On	VDIMAH	EN/DIM Terminal	2.98			V
Digital Dim Maximum Input Low	VDIMDL	EN/DIM Terminal			200	mV
Digital Dim Minimum Input High	VDIMDH	EN/DIM Terminal	2.98			V
EN Sleep Maximum Input Low	EN_sleep	EN/DIM Terminal			200	mV
EN Pull-Up Current	IEN	EN/DIM Terminal	1.5	5	10	µA
EN Sleep Mode Timer	EN_timer	VEN = 0.6V to 0V Falling Edge -> Sleep	29	32.8		ms
Sleep Mode to Output Enabled Delay Time	Twake	VEN rising (0V to VDIMH) to VSW start switching			250	µs
5V Linear Regulator Voltage	VDD	VIN >= VDD_hr + max VDD, Idd <= Ivdd_max	4.75	5	5.25	V
VDD short circuit current	Ivdd_sckt	VDD shorted to ground			40	mA
Under Voltage Lockout Rising Threshold	UVLO_rise	VIN Terminal		4.25	4.5	V

Parameter	Symbol	Condition	Min	Typ	Max	Units
Under Voltage Lockout Falling Threshold	UVLO_fall	VIN Terminal	4	4.1		V
Under Voltage Lockout Threshold Hysteresis	UVLO_hys	VIN Terminal		150		mV
Thermal Shutdown	TSD	Die Temperature	140			ºC

5 Pin Functions

Pin	Name	Description
1	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
2	VDD	Slave output of the internal linear regulator of voltage VDD. Connect a 1µF capacitor from this pin to ground. VIN needs to exceed the VDD_minVIN spec in order for the VDD output to be in spec.
3	GND	Ground. (Note: Connect the exposed heat slug on package backside to GND.)
4	SW	Switching Output. SW is the switching node that drives the external inductor. A suitable Schottky diode must be connected between SW (anode) and IN (cathode).
5	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switch. Drive VIN with a power source in the specified operational range. Bypass VIN to GND with a suitably large, high frequency capacitor to supply switching current to the IC.
6	CSP	Current Sense Input Positive. CSP is the voltage reference for the current sense input. Connect CSP to the current sense resistor on the decoupling capacitor side, and route differentially with CSN to help reject noise. Due to the finite common mode rejection of the CSP/CSN amplifier, performance of the PS5610 will be negatively impacted by high frequency VCS common mode voltage changes.
7	CSN	Current Sense Input Negative. CSN senses the regulated output current. Connect CSN to the current sense resistor on the cathode side of the LED string. The differential voltage between CSP and CSN is defined by "VCS" in the Electrical Characteristics. Due to the finite common mode rejection of the CSP/CSN amplifier, performance of the PS5610 will be negatively impacted by high frequency VCS common mode voltage changes.
8	EN/DIM	Enable and PWM Dimming Signal Input. Puts the converter in sleep mode after EN/DIM is <"EN_sleep" for >"EN_timer." Also serves as a PWM dimming input for a signal adhering to the "Fpwm" spec. Diming can also be performed with a DC input between "VDIML" and "VDIMH" using the internal "Framp" oscillator.

6 Topology Configurations

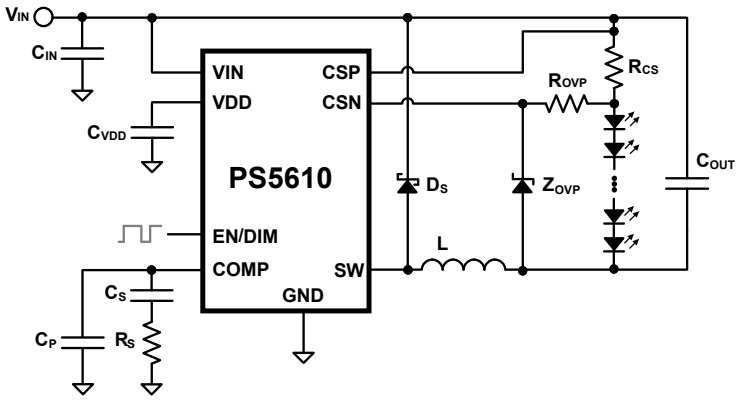


Figure 6.1: Buck Mode LED Driver

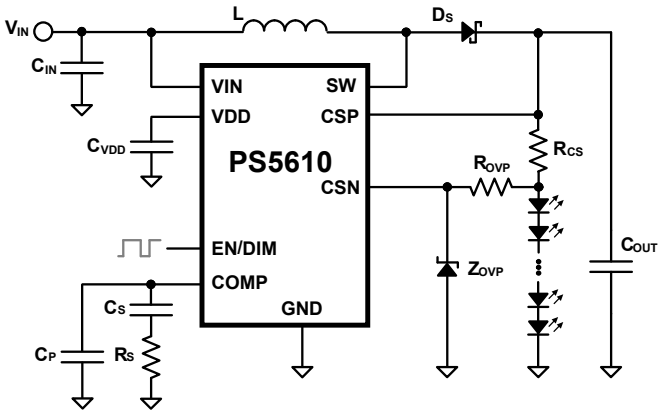


Figure 6.2: Boost Mode LED Driver

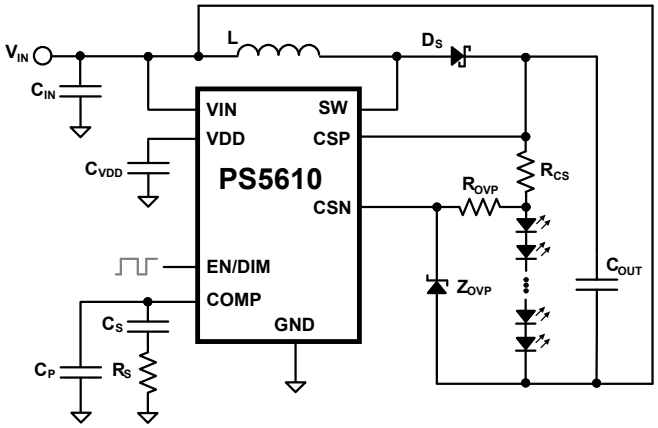


Figure 6.3: Buck-Boost Mode LED Driver

7 Block Diagram

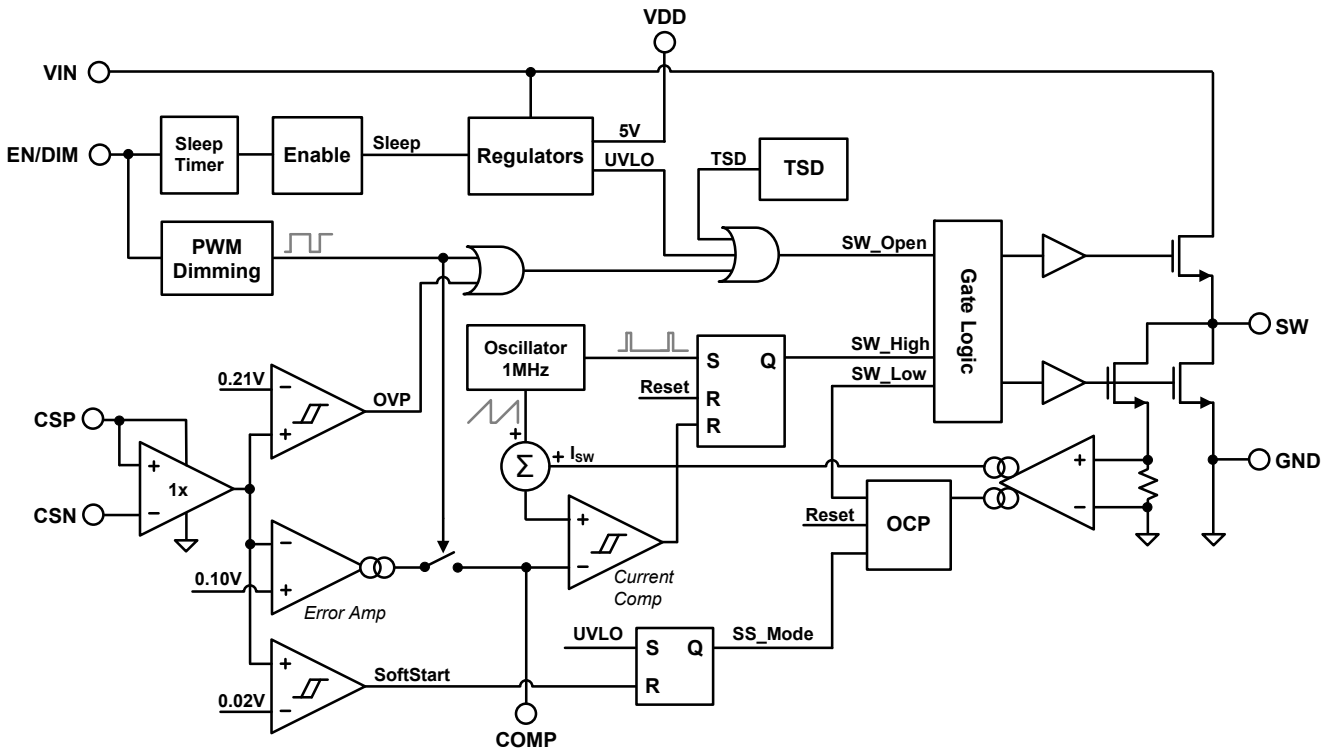


Figure 7.1: Functional Block Diagram

8 Functional Description

8.1 Modes of Operation

The PS5610 has four distinct modes of operation.

- Digital LED Dimming Mode
  - EN/DIM is given a PWM signal adhering to the specifications above. Digital low is less than VDIMDL and digital high is greater than VDIMDH.
- Analog LED Dimming Mode
  - EN/DIM is supplied with a voltage in the range of VDIMAL to VDIMAH.
- Default Mode
  - EN/DIM is left disconnected. The PS5610 will supply the current for which it was configured.
- Sleep Mode
  - EN/DIM is held below EN_sleep for greater than EN_timer.
  - A UVLO event is triggered.

Figure 8.1 outlines the different areas of operation.

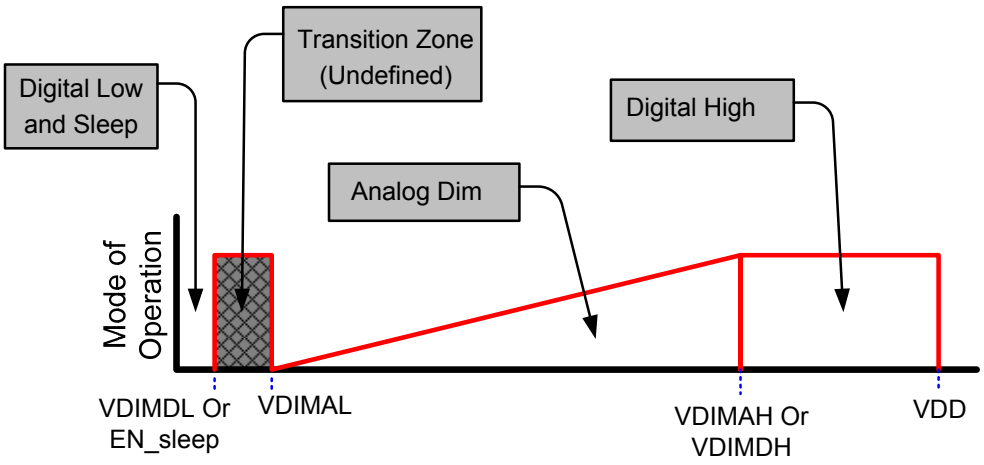


Figure 8.1: EN/DIM Modes of Operation

8.2 Shared Enable and Dim Functionality

To reduce the PS5610 pin count the EN (enable) and DIM functions are combined into one pin. The EN function turns the majority of the circuitry off (sleep mode) to achieve the "IQoff" supply current. The DIM function enables and disables the output stage using a PWM input to realize LED dimming. When the PS5610 is in DIM mode, the supply current is "IQ2." To combine these two functions a timer has been added such that the PS5610 enters sleep mode after the EN/DIM pin has been below "EN_sleep" for the duration of "EN_timer" as specified in the Electrical Characteristics section of this document. Thus, when a PWM signal, in the range of "Fpwm," is applied to EN/DIM the PS5610 will modulate the output stage but will not enter sleep mode; this is illustrated below.

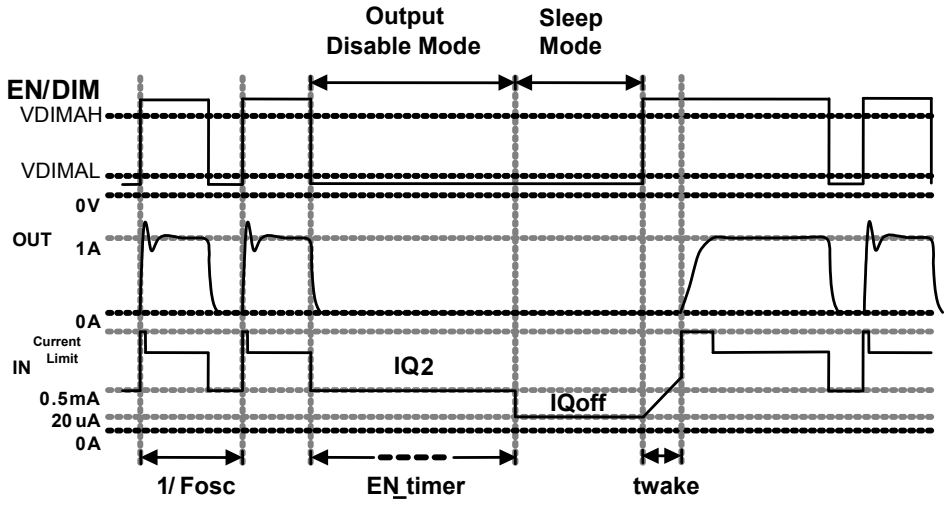


Figure 8.2: Timing Diagram for Enable

8.3 Startup

Changing the state of operation from Sleep to Enabled happens when the EN/DIM input is driven high. Because the device was asleep, it takes a short period of time defined by “Twake” to reinitialize the circuitry and to start normal operation.

Once awake, the SW pin will begin switching with the minimum on time, “Ton_min,” until the Vcomp voltage requests a peak current that is higher than the minimum on time. The compensation ramps slowly due to the maximum output current of the error amplifier and the compensation capacitance. Eventually the peak current requested by Vcomp will rise above the current limit threshold “IS1.” The peak current will remain at “IS1” until the output capacitor (C_{OUT}) has been fully charged. The LED output current (I_{OUT}) will not start rising until the output capacitor (C_{OUT}) has been charged enough to forward bias the LED string. Once the LEDs are forward biased the control loop will close and regulate the current as defined by the current set resistor Rcs. The average inductor current will become equal to the output current (I_{OUT}).

The startup of the PS5610 is detailed in Figure 8.3 below.

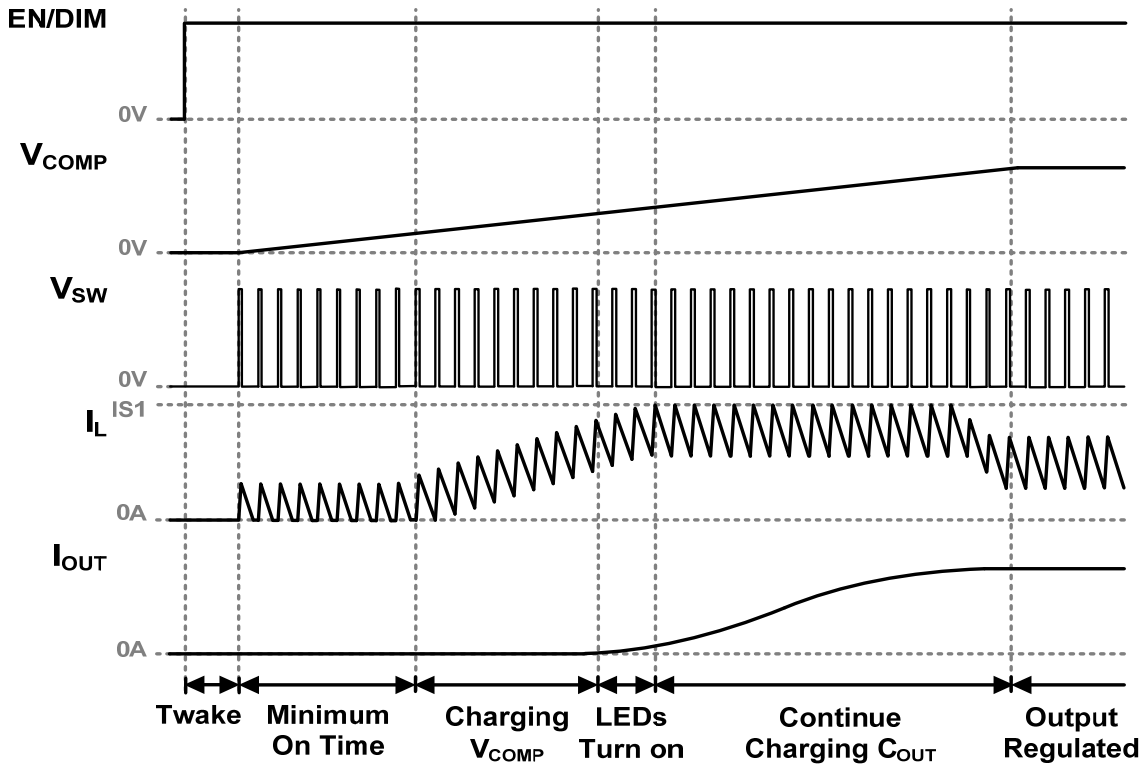


Figure 8.3: Startup Waveforms

8.4 Analog LED Dimming

Analog LED dimming can be achieved by applying a DC voltage (in the “VDIML” to “VDIMH” range) to the EN/DIM pin. This analog DIM voltage is compared against an internal saw tooth waveform of frequency Framp, with a “Dpwm_res” resolution, creating the PWM signal that drives the LED, as illustrated below in Figure 8.4.

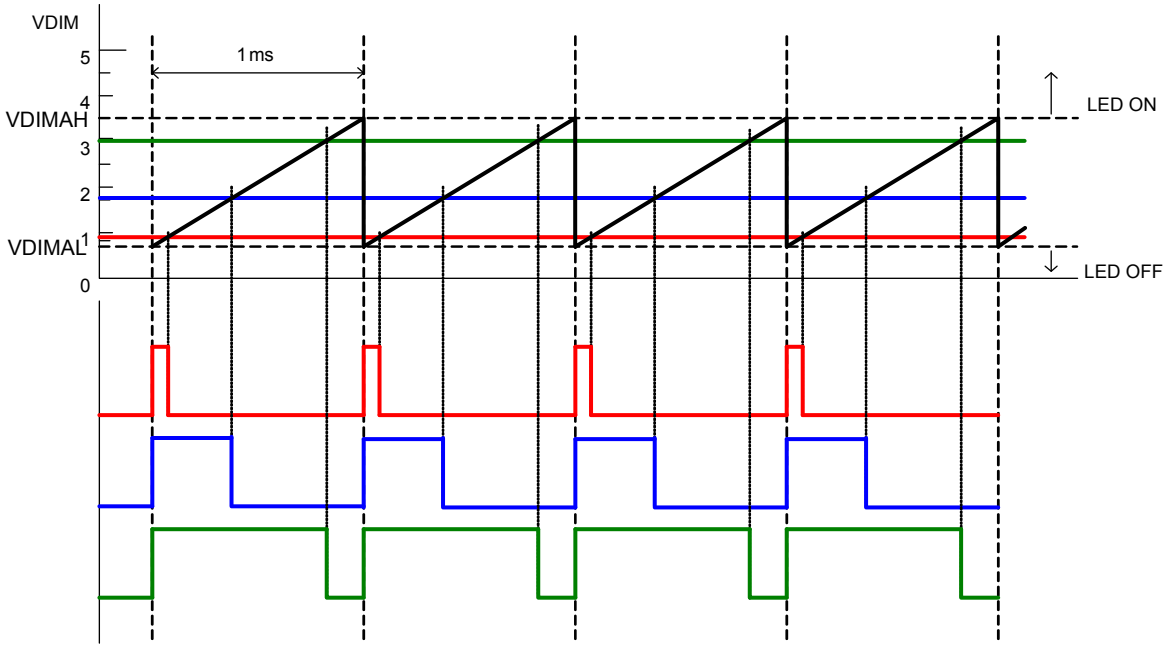


Figure 8.4: Analog LED Dimming Functionality

When transitioning EN/DIM from below the EN_sleep threshold into the analog LED dimming range between VDIML and VDIMH, the PS5610 will append 8 pulses to the beginning of the first pulse group. For example, when stepping the EN/DIM pin to a voltage that normally generates 16 pulses the first group will have 24 pulses, as illustrated in Figure 8.5.

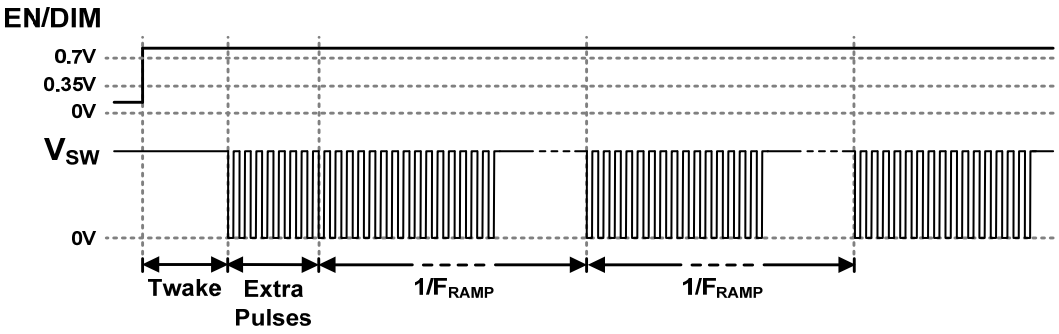


Figure 8.5: Analog Dim Startup Waveforms (not to scale)

8.5 Digital LED Dimming

Digital LED dimming can support much higher dimming ratios than analog dimming. Digital dimming is controlled by a PWM signal applied to the EN/DIM pin. The frequency of this digital PWM signal must be in the range of “Fpwm”. Current output is disabled when EN/DIM is less than “VDIMDL” and enabled when greater than “VDIMDH”. When dimming digitally, please observe the appropriate “Tpwm” specification limits.

In output disabled mode (EN/DIM low) the SW pin becomes high impedance and the part consumes “IQ2” of quiescent current. The output current (I_{OUT}) will not instantly go to zero but will be held up by the output capacitor (C_{OUT}). During this off time the capacitor is depleted only enough to turn off the string of LEDs and the error amplifier is disconnected from the COMP pin. This stores the previous state of the compensation network instead of driving it to the rail, allowing the converter to quickly return to its operating point when the PWM signal returns high. Some ringing will occur at the SW pin when disabled due to parasitic capacitance and the inductance at the switch node; however, this ringing is common and is not a problem due to its low energy content.

When EN/DIM changes from “disabled” to “enabled” the next cycle will begin. There will be a delay of “TD” before the output drive restarts. Once the output drive starts, it will momentarily supply a higher current than defined by the current set resistor Rcs, up to the “IS1” current limit, to recharge the output capacitor and quickly return to regulation.

Figure 8.6 illustrates the digital LED diming operation with a PWM input. Please note, a very short off-time is shown. Off times shorter than “Tpwm_minOff” can result in non-linear loop behavior and unwanted visual effects.

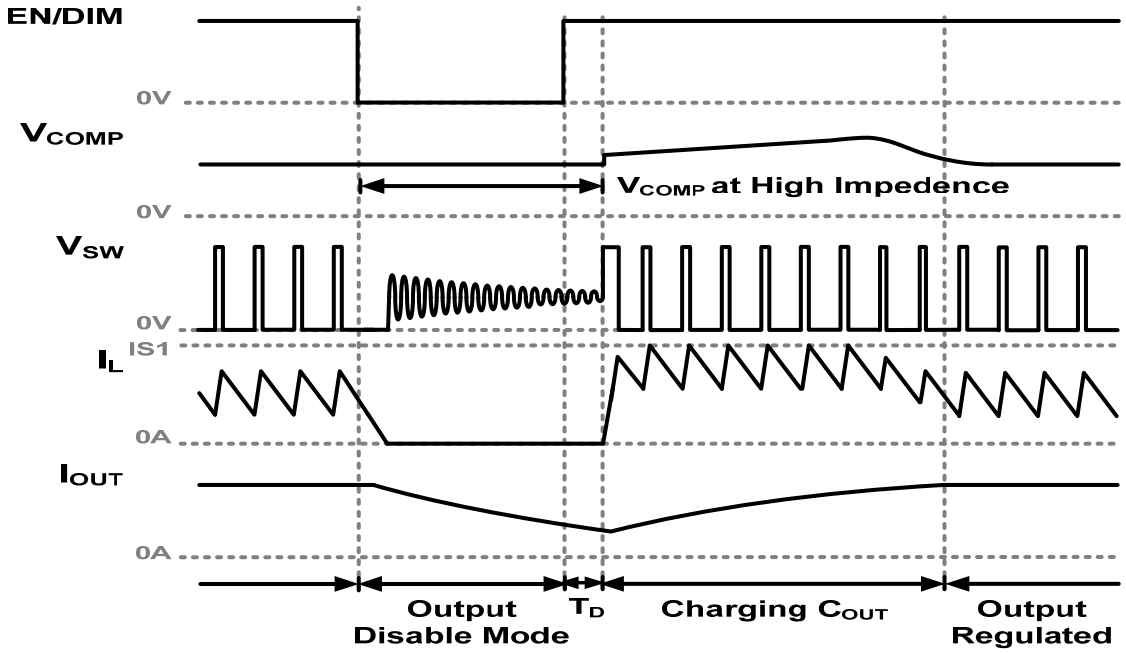


Figure 8.6: Output Dimming Waveforms

8.6 Over Current Protection

The PS5610 includes an internal OCP (over current protection) circuit which prevents the peak current from exceeding "IS1," as illustrated in Figure 8.7. This is done to protect the IC in the case of a failure or output short. After the current returns to a proper operating range the PS5610 will automatically return to normal operation. OCP behavior is illustrated in Figure 8.8.

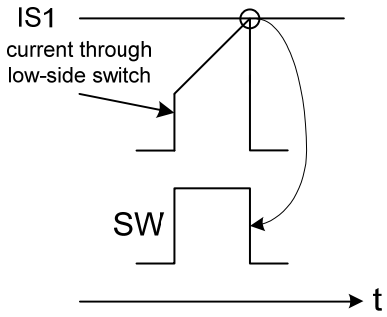


Figure 8.7: IS1 Definition

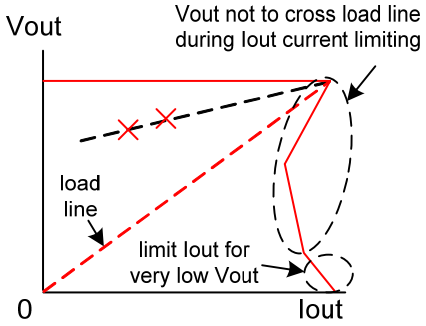


Figure 8.8: OCP Behavior

8.7 Over Voltage Protection

In the case of an LED failing open the control loop would cause the output voltage to rise up, out of regulation. In many buck converter applications this failure is acceptable; however if the output components are not rated for the input voltage or the PS5610 is configured in boost or buck-boost modes it will be necessary to add two external components to realize over voltage protection.

In the Typical Implementation schematic (page 1), R_{OVP} and Z_{OVP} implement the over voltage protection and can be removed if overvoltage protection is not required. In the case of an LED failing open the Zener diode (Z_{OVP}) will conduct and in conjunction with R_{OVP} will cause the current sense voltage (CSP-CSN) to rise. Note that, due to the CSN pin input current, the use of R_{OVP} will result in a (typically small) regulation error of (I_{CSN}* R_{OVP})/100mV. The reverse break down voltage of Z_{OVP} must be greater than the total maximum voltage drop across the string of LEDs.

8.8 Line Regulation

The PS5610 is a current regulator where the load is generally a string of LEDs that can be approximately modeled as a voltage source. The quality of the line regulation is a function of how much the regulated current (I_{OUT}) changes as the input supply voltage changes. Voltage regulators are generally able to keep the output voltage regulated within 0.3% nominal and 0.6% maximum. Therefore, when the regulated current is 1A the line regulation should be 3mA nominal and 6mA maximum.

A fixed output voltage of 7.5V is selected to mimic two LEDs connected in series. The input supply voltage is swept between 12V and 55V to meet the minimum on time and maximum duty cycle requirements.

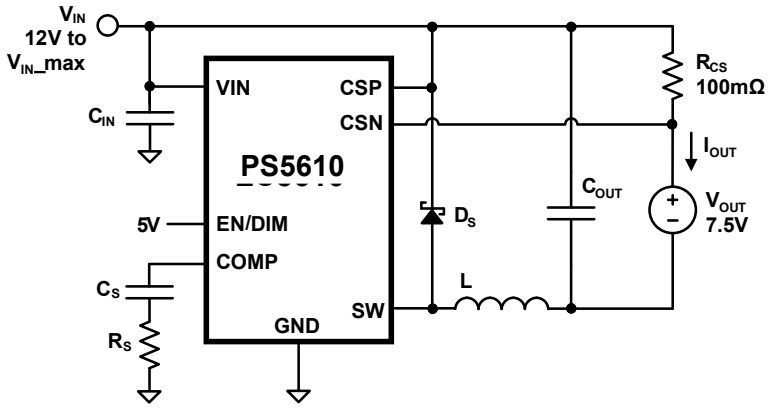


Figure 8.9: Line Regulation Test Setup

8.9 Load Regulation

The PS5610 is a current regulator where the load is generally a string of LEDs that can have a forward voltage variation of more than 30%. Since a string of LEDs can be approximately modeled as a voltage source the quality of the load regulation is a function of how much the regulated current (I_{OUT}) changes as the output voltage source changes. Voltage regulators are generally able to keep the output voltage regulated within 0.3% nominal and 0.6% maximum. Therefore, when the regulated output current is 1A the load regulation should be 3mA nominal and 6mA maximum.

To test for the worst case condition an input supply voltage of VIN_max is selected. To exercise the full range of the regulator the output voltage source is swept between (Ton_min*Fosc*VIN_max) and (Dmax*VIN_max) to meet the minimum on time and maximum duty cycle requirements.

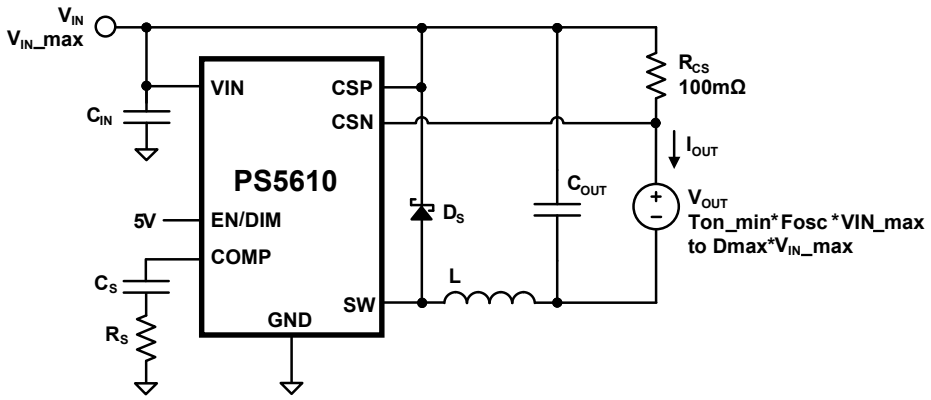


Figure 8.10: Load Regulation Test Setup

9 Component Selection

See the “Electrical Characteristics” table starting on page 2, to find actual values of various parameters referred to in this section. Please note some equations are repeated for clarity and readability.

There are two items to think about while designing the circuit:

(1) The power diode voltage drop may need to be taken into account at low output voltages (Vout).

(2) The LED resistance is important in calculating proper output capacitance values. Some suggested starting points are:

a. Red, Orange, Yellow: 0.40V / Itest

b. Green: 0.44V / Itest

c. Blue, White: 0.34V / Itest

where Itest is the test current specified by the manufacturer.

9.1 Buck Mode

V_{OUT} Calculation

V_{OUT} is defined by the LED forward voltage (V_{FWD}), number of LEDs (n), and the current sense voltage (V_{CS}):

$$V_{OUT} = n \cdot V_{FWD} + V_{CS} \qquad (V_{OUT} \text{ definition})$$

Duty Cycle Constraints

The output voltage (V_{OUT}) must result in a duty cycle (D) that falls between the minimum duty cycle (defined by the minimum on time divided by the switching period) and maximum duty cycle:

$$Ton\_min \cdot Fosc < D < Dmax \qquad \text{(duty cycle requirement)}$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \qquad \text{(buck mode)}$$

Simplified Power-In to Power-Out Relationship

Using the simplifying assumption that the PS5610 is 100% efficient (that is, power in = power out), the following relationship is useful for calculating one variable in terms of the other three:

$$V_{IN} \bullet I_{IN} = V_{OUT} \bullet I_{OUT}$$

Regulated LED Current Selection

The regulated output current is selected by sizing the R_{CS} resistor connected between the CSP and CSN pins as:

$$I_{OUT} = \frac{V_{CS}}{R_{CS}}$$

Inductor Selection

For a buck mode converter

$$I_L = I_{OUT}$$ (buck mode inductor current relationship)

For a given input voltage, output voltage, and oscillator frequency the inductor value will determine the peak-to-peak inductor current ripple. A good starting place for the inductor ripple current is (see Figure 9.1).

$$\Delta I_L \approx 0.4 I_L$$ (inductor current ripple rule of thumb)

In most cases it is undesirable to exceed a ripple value of 0.4 and lower values offer better performance.

To ensure the current limiting does hinder the regulated output current the current ripple should be selected such that it does not exceed I_{S1} (see Figure 9.1).

$$\Delta I_L < 2(I_{S1} - I_{OUT})$$ (current limit requirement)

It is also important that the ripple current does not go negative because when the ripple current is negative the external diode will not conduct and the full inductor current will pass through the 70Ω high side switch. The high side switch is designed as a pull-up switch and will be very inefficient if it carries the inductor current. To prevent the high side switch from conducting negative current the current ripple should be selected such that it does not exceed (see Figure 9.2).

$$\Delta I_L < 2\ I_{OUT}$$ (positive inductor current requirement)

Proper sizing of the regulated current and the ripple current is illustrated in Figure 9.1. Figure 9.2 illustrates the case where regulated current (I_{OUT}) is too small or the ripple current (ΔI_L) is too large, which will cause the PS5610 to be very inefficient.

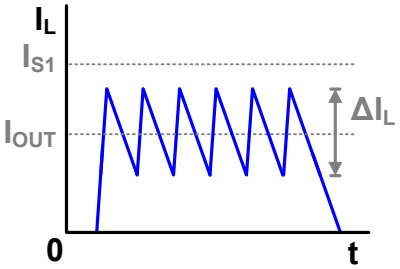


Figure 9.1: Proper Regulated Current and Inductor Selection

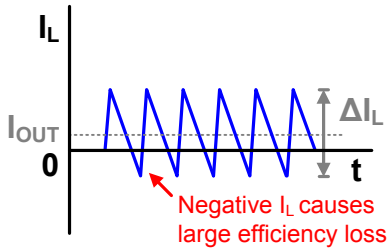


Figure 9.2: Improper Regulated Current and Inductor Selection

After an appropriate ripple current magnitude has been selected the required inductance is determined from the following equation:

$$L = \frac{1}{\Delta I_L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\frac{1}{F_{OSC}}$$ (buck mode inductor selection)

where Vout is the voltage drop across the LED string.

It is important to select an inductor that will not saturate under the maximum peak inductor current derived below.

$$I_{SAT} > I_{OUT} + \frac{1}{2}\Delta I_L$$ (inductor minimum saturation current)

When operating with duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$) the inductor should also satisfy the following relationship, where "m_a" is the PS5610's slope compensation value:

$$\left|\frac{V_{OUT} - m_a L}{V_{IN} - V_{OUT} + m_a L}\right| < 1$$ (buck mode slope compensation requirement)

Output Capacitor Selection

The PS5610 uses a basic current mode control loop to regulate the output current. Current mode control regulates by generating an error between the output regulation and a reference and this error sets the peak inductor current that will reset the switch node. This method requires both feedback of the output current (I_{OUT}) and inductor current (I_L). The PS5610 uses an internal current sense to detect the inductor current (I_L) and an external current sense to detect the output current (I_{OUT}), as detailed in Figure 9.3. With this configuration the PS5610 can accommodate an output capacitor (C_{OUT}) across the LED string. As the output capacitor (C_{OUT}) changes, the compensation network (C_S and R_S) must change so that the error amp generates a low frequency error signal.

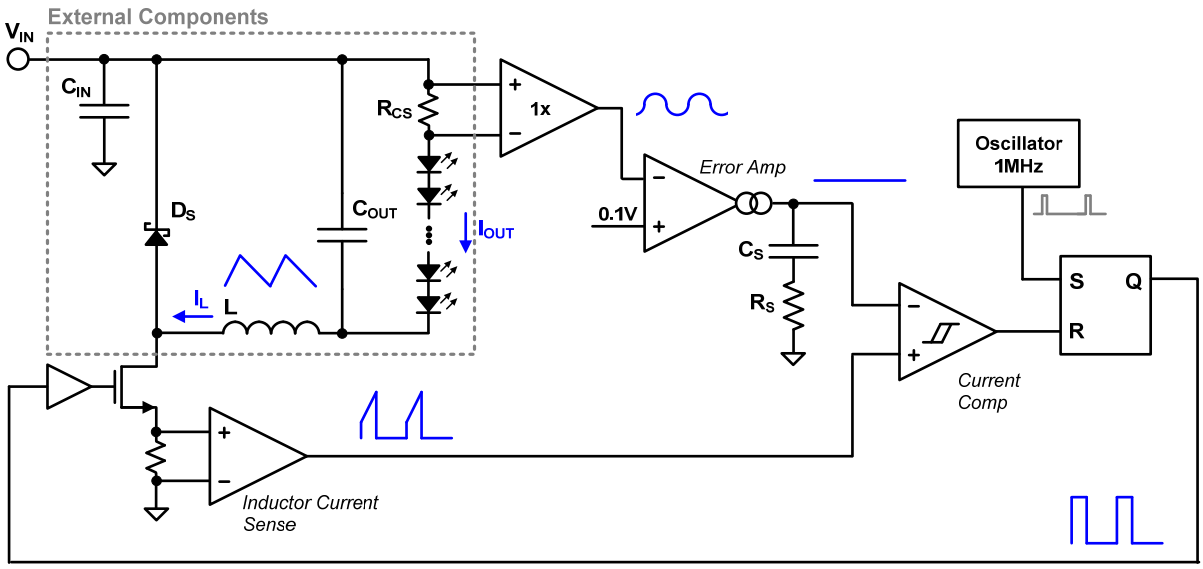


Figure 9.3: Buck Mode Control Loop Flow Diagram

For the buck mode configuration, the output capacitor (C_{OUT}) is optional because the CCM inductor current flows through the LED string. Having a small (or no) C_{OUT} enables the highest dimming ratios at the expense of higher ripple current through the LED string.

The output capacitor (C_{OUT}) reduces the output current ripple (ΔI_{OUT}) through the LED string but increases the fall time of the output current during PWM dimming. Thus the output capacitor must be carefully selected such that it filters only the necessary amount of current ripple.

C_{OUT} Selection for Buck Mode

The output current ripple can be derived by comparing the capacitor and diode small signal resistance for the given

operating point. The capacitor equivalent resistance (R_{COUT}) of the output capacitor (C_{OUT}), assuming a triangular inductor current ripple and a fixed frequency (f), is given by:

$$R_{COUT} = \frac{1}{8 f C_{OUT}} \qquad \text{(capacitor equivalent resistance)}$$

The resistance of the LED string is given by:

$$R_{LED} = n\frac{\Delta V}{\Delta I} \qquad \text{(LED equivalent resistance)}$$

where $\Delta V/\Delta I$ is obtained from the V-I curve in the LED's datasheet.

The output network can then be model as a resistor current divider resulting in the following relationship for the output current ripple (ΔI_{OUT}) given the inductor current ripple (ΔI_L):

$$\Delta I_{OUT} = \frac{\Delta I_L}{1 + \frac{R_{LED}}{R_{COUT}}} \qquad \text{(buck mode output current ripple model)}$$

Buck Mode Control Loop Compensation Theory

The following equations govern the compensation loop in buck mode:

$$A_{VDC} = R_{CS} G_{CS} A_{EA} \qquad \text{(buck mode DC loop voltage gain)}$$

$$f_{P1} = \frac{G_{EA}}{2\pi C_S A_{EA}} \qquad \text{(buck mode compensation pole)}$$

$$f_{P2} = \frac{1}{2\pi C_{OUT}(R_{CS} + R_{LED})} \qquad \text{(buck mode output network pole)}$$

$$f_{Z1} = \frac{1}{2\pi C_S R_S} \qquad \text{(buck mode compensation zero)}$$

Buck Mode Compensation Network Selection

When selecting the compensation network, either a capacitor (Cp) or a resistor and capacitor (Rs and Cs) combination must be selected. Please select the appropriate network based on the output capacitor (Cout). For a large Cout, where Cout creates an output pole that is much lower than the switching frequency (Fosc), calculate Cp. For a small or nonexistent Cout, calculate Rs and Cs.

Buck Mode Pole-Zero Compensation (large C_{OUT})

When using a large output capacitor (C_{OUT}) to reduce the LED current ripple, the output network pole (f_{P2}) becomes a low frequency pole and must be compensated with a zero. Pole-zero compensation is most reliable when the output network pole (f_{P2}) is below the compensation zero ($f_{P2} < f_{Z1}$). With pole-zero compensation the zero (f_{Z1}) sets the phase margin and the dominant compensation pole (f_{P1}) sets the crossover frequency (f_C).

The crossover frequency (f_C) should be set at about one-tenth the switching frequency (f_{OSC}). Setting the crossover

frequency (f_C) too high can cause the system to become unstable and setting it too low can result in a slower transient response. The compensation resistor (R_S) sets the crossover frequency independent of the compensation capacitor (C_S). Thus the following formula can be used to select the compensation resistor (R_S):

$$R_S = \frac{2\pi C_{OUT} f_C}{G_{EA} G_{CS}} \left(1 + \frac{R_{LED}}{R_{CS}}\right)$$ (buck mode pole-zero compensation resistor selection)

Unfortunately the crossover frequency (f_C) is impacted by the LED equivalent resistance (R_{LED}), which can vary significantly, thus the crossover frequency (f_C) must be chosen with margin.

Since the dominant compensation pole (f_{P1}) and the output network pole (f_{P2}) are much lower than the crossover frequency (f_C) they each contribute 90° of phase at the crossover frequency (f_C). Thus the phase margin (PM) is set by the ratio of the crossover frequency (f_C) and the compensation zero (f_{Zq}), as follows:

$$PM_R = \frac{f_C}{f_{Z1}} = \tan(PM)$$ (buck mode pole-zero compensation phase margin ratio)

A phase margin ratio (PM_R) of 4 sets the phase margin at about 76° and is set by the compensation capacitor (C_S) as detailed in the following formula:

$$C_S = \frac{PM_R}{2\pi R_S f_C}$$ (buck mode pole-zero compensation capacitor selection)

Buck Mode Dominant Pole Compensation (no or small C_{OUT})

As discussed in the output capacitor selection section, the highest dimming ratios can be achieved with no or a small output capacitor (C_{OUT}). With this case the output network pole (f_{P2}) is located beyond the crossover frequency (f_C) making the system a single pole system. Thus the crossover frequency is simply set by the dominant pole realized with the compensation capacitor (C_P) as follows:

$$C_P = \frac{G_{EA} G_{CS} R_{CS}}{2\pi f_C}$$ (buck mode dominant pole compensation capacitor selection)

As the output network pole (f_{P2}) approaches the cross over frequency (f_C) the phase margin will be reduced. To provide proper phase margin (PM) ensure that the output network pole (f_{P2}) and the crossover frequency (f_C) abide by the following relationship:

$$f_{P2} > \frac{f_C}{\tan(90° - PM)}$$ (buck mode dominant pole phase margin)

The best line and load regulation will be achieved when setting the crossover frequency (f_C) at about one-tenth the switching frequency (f_{OSC}). However, when exiting output disable mode the output will slew to restore the output capacitor voltage and the LED current. During this period of time the error amplifier is saturated; thereby driving the compensation capacitor (C_S) away from the stored operating point. This situation will cause the LED current to overshoot as the error amplifier drives the compensation capacitor (C_S) back to the proper operating point. To reduce this effect the compensation capacitor (C_S) can be made larger by lowering the crossover frequency (f_C), which will reduce the magnitude the compensation network is driven away from its proper operating point. The crossover frequency (f_C) can be optimized based on the following relationship:

$$f_c = \frac{f_{P2}}{K_{DAMP}}$$ (buck mode dominant pole crossover frequency damping)

The above relationship shows that the crossover frequency can be scaled with the output network pole (f_{P2}) to achieve the same overshoot characteristic. In addition, increasing the damping constant (K_{DAMP}) will reduce the overshoot. The damping constant can range from about 5 to 50 and typically a value of 25 gives a good response.

9.2 Boost Mode

V_{OUT} Calculation

V_{OUT} is defined by the LED forward voltage (V_{FWD}), number of LEDs (n), and the current sense voltage (V_{CS}):

$$V_{OUT} = n \cdot V_{FWD} + V_{CS}$$ (V_{OUT} definition)

Duty Cycle Constraints

The output voltage (V_{OUT}) must result in a duty cycle (D) that falls between the minimum duty cycle (defined by the minimum on time divided by the switching period) and maximum duty cycle:

$$Ton\_min \cdot Fosc < D < Dmax$$ (duty cycle requirement)

where

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$ (boost mode)

Simplified Power-In to Power-Out Relationship

Using the simplifying assumption that the PS5610 is 100% efficient (that is, power in = power out), the following relationship is useful for calculating one variable in terms of the other three:

$$V_{IN} \bullet I_{IN} = V_{OUT} \bullet I_{OUT}$$

Regulated LED Current Selection

The regulated output current is selected by sizing the R_{CS} resistor connected between the CSP and CSN pins:

$$I_{OUT} = \frac{V_{CS}}{R_{CS}}$$

Inductor Selection

For a boost mode converter

$$I_L = I_{IN}$$ (boost mode inductor current relationship)

For a given input voltage, output voltage, and oscillator frequency the inductor value will determine the peak-to-peak inductor current ripple. A good starting place for the inductor ripple current is (see Figure 9.1):

$$\Delta I_L \approx 0.4 I_L$$ (inductor current ripple rule of thumb)

In most cases it is undesirable to exceed a ripple value of 0.4 and lower values offer better performance.

To ensure the current limiting does hinder the regulated output current the current ripple should be selected such that

it does not exceed I_{S1} (see Figure 9.1):

$$\Delta I_L < 2(I_{S1} - I_{OUT}) \qquad \text{(current limit requirement)}$$

Proper sizing of the regulated current and the ripple current is illustrated in Figure 9.1. Figure 9.2 illustrates the case where regulated current (I_{OUT}) is too small or the ripple current (ΔI_L) is too large, which will cause the PS5610 to be very inefficient.

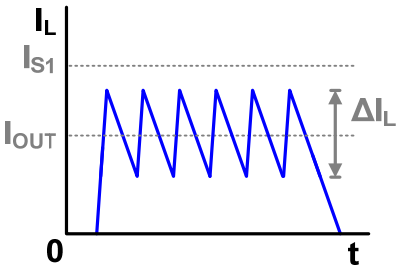


Figure 9.1: Proper Regulated Current and Inductor Selection

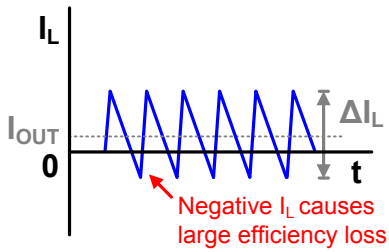


Figure 9.2: Improper Regulated Current and Inductor Selection

After an appropriate ripple current magnitude has been selected the required inductance is determined from the following equation:

$$L = \frac{1}{\Delta I_L} V_{IN}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)\frac{1}{F_{OSC}} \qquad \text{(boost mode inductor selection)}$$

where Vout is the voltage drop across the LED string.

It is important to select an inductor that will not saturate under the maximum peak inductor current derived below:

$$I_{SAT} > I_{OUT} + \frac{1}{2}\Delta I_L \qquad \text{(inductor minimum saturation current)}$$

When operating with duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5) the inductor should also satisfy the following relationship, where "m_a" is the PS5610's slope compensation value:

$$\left|\frac{V_{OUT} - V_{IN} - m_a L}{V_{IN} + m_a L}\right| < 1 \qquad \text{(boost mode slope compensation requirement)}$$

Because the inductor is responsible for a zero in the control loop equations, the chosen inductor value must be checked for stability as shown in the "Boost Mode Compensation Network Selection."

Output Capacitor Selection

The PS5610 uses a basic current mode control loop to regulate the output current. Current mode control regulates by generating an error between the output regulation and a reference and this error sets the peak inductor current that will reset the switch node. This method requires both feedback of the output current (I_{OUT}) and inductor current (I_L). The PS5610 uses an internal current sense to detect the inductor current (I_L) and an external current sense to detect the output current (I_{OUT}), as detailed in Figure 9.3. With this configuration the PS5610 can accommodate an output

capacitor (C_{OUT}) across the LED string. As the output capacitor (C_{OUT}) changes, the compensation network (C_S and R_S) must change so that the error amp generates a low frequency error signal.

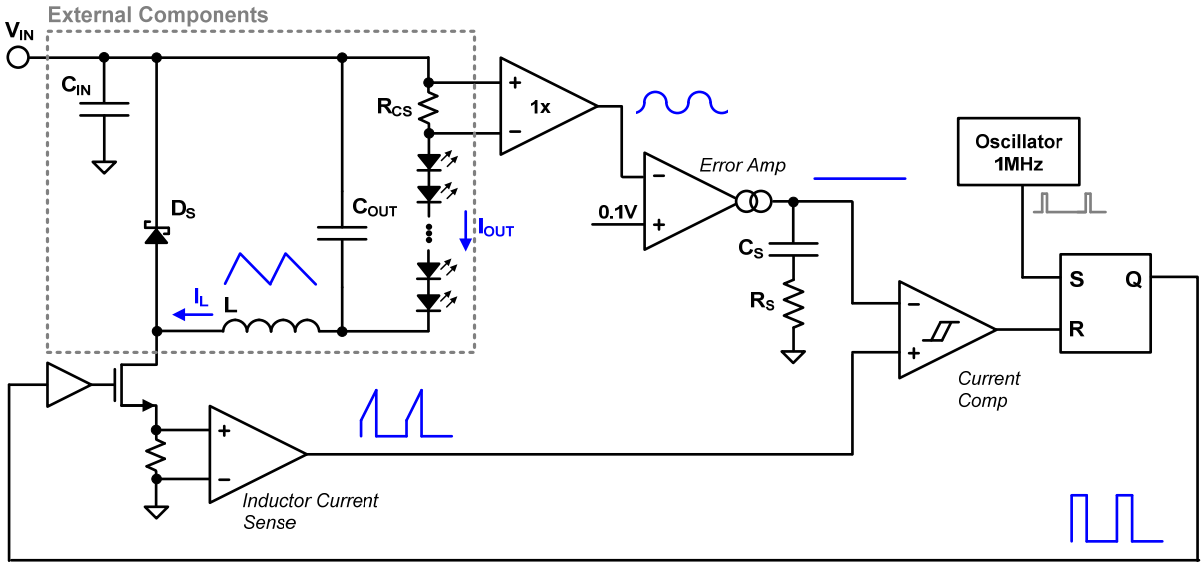


Figure 9.3: Buck Mode Control Loop Flow Diagram

For the boost mode configuration, C_{OUT} is required to prevent PWM (discontinuous) current flow through the LED string. C_{OUT} removes the high frequency components from the PWM current waveform, resulting in a continuous current flowing through the LED string.

The output capacitor (C_{OUT}) reduces the output current ripple (ΔI_{OUT}) through the LED string but increases the fall time of the output current during PWM dimming. Thus the output capacitor must be carefully selected such that it filters only the necessary amount of current ripple.

C_{OUT} Selection for Boost Mode

The desired output capacitor can be directly calculated from the output current ripple (ΔIout):

$$\Delta I_{OUT} = \frac{I_{OUT} D}{C_{OUT} R_{OUT} F_{OSC}}$$ (boost mode output current ripple model)

$$C_{OUT} = \frac{I_{OUT} D}{\Delta I_{OUT} R_{OUT} F_{OSC}}$$ (boost mode output capacitor calculation)

Boost Mode Control Loop Compensation Theory

The following equations govern the compensation loop in boost mode:

$$A_{VDC} = \tfrac{1}{2}(1-D) R_{CS} G_{CS} A_{EA}$$ (boost mode DC voltage gain)

$$f_{P1} = \frac{G_{EA}}{2\pi C_P A_{EA}}$$ (boost mode compensation pole)

$$f_{P2} = \frac{1}{2\pi C_{OUT}(R_{CS} + R_{LED})}$$ (boost mode output network pole)

$$f_{Z1} = \frac{(R_{LED} + R_{CS})(1-D)^2}{2\pi L}$$ (boost mode compensation zero)

Boost Mode Compensation Network Selection

The boost mode control loop zero ($f_{Z1)}$ is a function of the inductor.

The second control loop pole (f_{P2})is a function of C_{OUT}.

The first control loop pole f_{P1} is set by the compensation capacitor:

$$C_P = \frac{G_{EA} G_{CS} R_{CS} L}{2\pi f_C C_{OUT}(R_{CS} + R_{LED})^2} \frac{V_{OUT}}{V_{IN}}$$ (boost mode compensation capacitor selection)

For stability, the control loop bandwidth must be adjusted to be less than the crossover frequency which leads to the following requirement:

$f_{P2} < f_C$ (control loop bandwidth requirement)

The following equations calculate phase margin

$$PM = 180° - \tan^{-1}\left(\frac{f_C}{f_{P1}}\right) - \tan^{-1}\left(\frac{f_C}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (general boost mode phase margin)

Assuming $f_{P1} << f_C$, then

$$PM = 90° - \tan^{-1}\left(\frac{f_C}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (simplified boost mode phase margin)

Assuming f_{P1} and f_{P2} are both much lower than crossover frequency, then

$$PM = \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (reduced boost mode phase margin)

9.3 Buck-Boost Mode

V_{OUT} Calculation

V_{OUT} is defined by the LED forward voltage (V_{FWD}), number of LEDs (n), and the current sense voltage (V_{CS}):

$V_{OUT} = n \cdot V_{FWD} + V_{CS}$ (V_{OUT} definition)

Duty Cycle Constraints

The output voltage (V_{OUT}) must result in a duty cycle (D) that falls between the minimum duty cycle (defined by the minimum on time divided by the switching period) and maximum duty cycle:

$$Ton\_min \cdot Fosc < D < Dmax \qquad \text{(duty cycle requirement)}$$

where

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} \qquad \text{(buck-boost mode)}$$

Simplified Power-In to Power-Out Relationship

Using the simplifying assumption that the PS5610 is 100% efficient (that is, power in = power out), the following relationship is useful for calculating one variable in terms of the other three:

$$V_{IN} \bullet I_{IN} = V_{OUT} \bullet I_{OUT}$$

Regulated LED Current Selection

The regulated output current is selected by sizing the R_{CS} resistor connected between the CSP and CSN pins:

$$I_{OUT} = \frac{V_{CS}}{R_{CS}}$$

Inductor Selection, Buck-Boost Mode

For a buck-boost mode converter

$$I_L = I_{IN} + I_{OUT} \qquad \text{(buck-boost mode inductor current relationship)}$$

For a given input voltage, output voltage, and oscillator frequency the inductor value will determine the peak-to-peak inductor current ripple. A good starting place for the inductor ripple current is (see Figure 9.1):

$$\Delta I_L \approx 0.4 I_L \qquad \text{(inductor current ripple rule of thumb)}$$

In most cases it is undesirable to exceed a ripple value of 0.4 and lower values offer better performance.

To ensure the current limiting does not hinder the regulated output current the current ripple should be selected such that it does not exceed I_{S1} (see Figure 9.1):

$$\Delta I_L < 2(I_{S1} - I_{OUT}) \qquad \text{(current limit requirement)}$$

It is also important that the ripple current does not go negative because when the ripple current is negative the external diode will not conduct and the full inductor current will pass through the 70Ω high side switch. The high side switch is designed as a pull-up switch and will be very inefficient if it carries the inductor current. To prevent the high side switch from conducting negative current the current ripple should be selected such that it does not exceed (see Figure 9.2):

$$\Delta I_L < 2\, I_{OUT} \qquad \text{(positive inductor current requirement)}$$

Proper sizing of the regulated current and the ripple current is illustrated in Figure 9.1. Figure 9.2 illustrates the case where regulated current (I_{OUT}) is too small or the ripple current (ΔI_L) is too large, which will cause the PS5610 to be very inefficient.

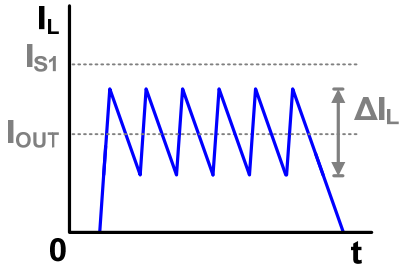


Figure 9.1: Proper Regulated Current and Inductor Selection

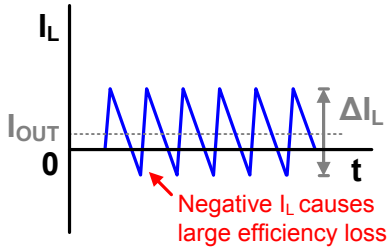


Figure 9.2: Improper Regulated Current and Inductor Selection

After an appropriate ripple current magnitude has been selected the required inductance is determined from the following equation:

$$L = \frac{1}{\Delta I_L}\left(\frac{V_{IN}V_{OUT}}{V_{IN}+V_{OUT}}\right)\frac{1}{F_{OSC}} \qquad \text{(buck-boost mode inductor selection)}$$

where Vout is the voltage drop across the LED string.

It is important to select an inductor that will not saturate under the maximum peak inductor current derived below.

$$I_{SAT} > I_{OUT} + \frac{1}{2}\Delta I_L \qquad \text{(inductor minimum saturation current)}$$

When operating with duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5) the inductor should also satisfy the following relationship, where "m_a" is the PS5610's slope compensation value:

$$\left|\frac{V_{OUT} - m_a L}{V_{IN} + m_a L}\right| < 1 \qquad \text{(buck-boost mode slope compensation requirement)}$$

Because the inductor is responsible for a zero in the control loop equations, the chosen inductor value must be checked for stability as shown in the "Buck-Boost Mode Compensation Network Selection."

Output Capacitor Selection

The PS5610 uses a basic current mode control loop to regulate the output current. Current mode control regulates by generating an error between the output regulation and a reference and this error sets the peak inductor current that will reset the switch node. This method requires both feedback of the output current (I_{OUT}) and inductor current (I_L). The PS5610 uses an internal current sense to detect the inductor current (I_L) and an external current sense to detect the output current (I_{OUT}), as detailed in Figure 9.3. With this configuration the PS5610 can accommodate an output capacitor (C_{OUT}) across the LED string. As the output capacitor (C_{OUT}) changes, the compensation network (C_S and R_S) must change so that the error amp generates a low frequency error signal.

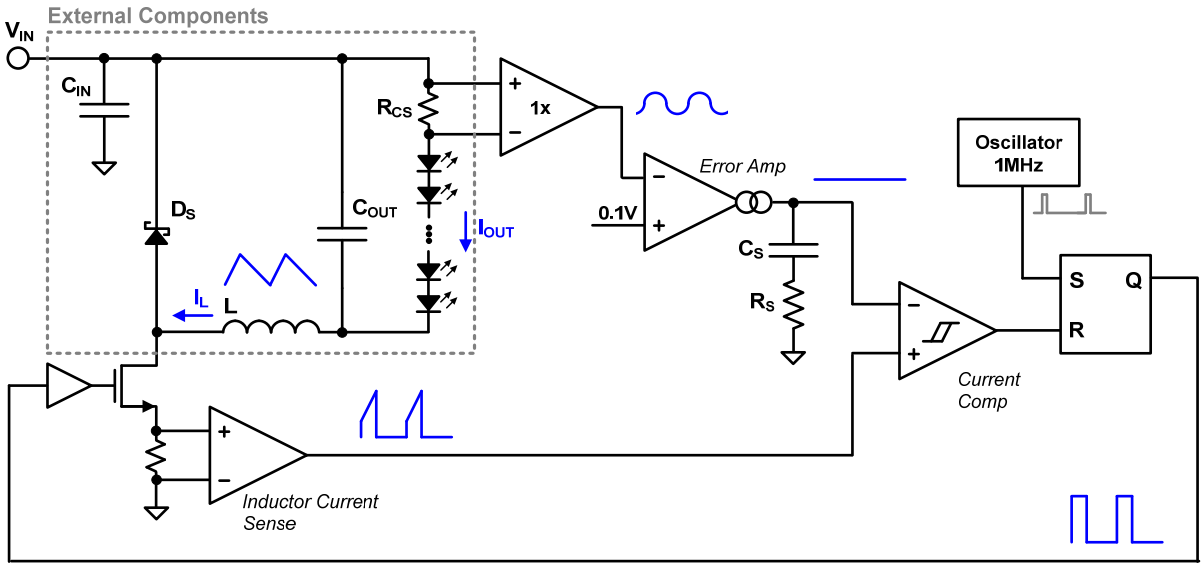


Figure 9.3: Buck Mode Control Loop Flow Diagram

For the buck-boost mode configuration, C_{OUT} is required to prevent PWM (discontinuous) current flow through the LED string. C_{OUT} removes the high frequency components from the PWM current waveform, resulting in a continuous current flowing through the LED string.

The output capacitor (C_{OUT}) reduces the output current ripple (ΔI_{OUT}) through the LED string but increases the fall time of the output current during PWM dimming. Thus the output capacitor must be carefully selected such that it filters only the necessary amount of current ripple.

C_{OUT} Selection for Buck-Boost Mode

The desired output capacitor can be directly calculated from the output current ripple (Δlout):

$$\Delta I_{OUT} = \frac{I_{OUT} D}{C_{OUT} R_{OUT} F_{OSC}}$$ (boost and buck-boost mode output current ripple model)

$$C_{OUT} = \frac{I_{OUT} D}{\Delta I_{OUT} R_{OUT} F_{OSC}}$$ (boost and buck-boost mode output capacitor calculation)

Buck-Boost Mode Control Loop Compensation Theory

The following equations govern the compensation loop in boost mode:

$$A_{VDC} = \tfrac{1}{2}(1-D) R_{CS} G_{CS} A_{EA}$$ (buck-boost mode DC voltage gain)

$$f_{P1} = \frac{G_{EA}}{2\pi C_P A_{EA}}$$ (buck-boost mode compensation pole)

$$f_{P2} = \frac{1}{2\pi C_{OUT}(R_{CS} + R_{LED})}$$ (buck-boost mode output network pole)

$$f_{Z1} = \frac{(R_{LED} + R_{CS})(1-D)^2}{2\pi L}$$ (buck-boost mode compensation zero)

Buck-Boost Mode Compensation Network Selection

The buck-boost mode control loop zero (f_{Z1}) is a function of the inductor.

The second control loop pole f_{P2} is a function of C_{OUT}.

The first control loop pole f_{P1} is set by the compensation capacitor:

$$C_P = \frac{G_{EA} G_{CS} R_{CS} L}{2\pi f_C C_{OUT}(R_{CS} + R_{LED})^2} \frac{V_{OUT}}{V_{IN}}$$ (buck-boost mode compensation capacitor selection)

For stability, the control loop bandwidth must be adjusted to be less than the crossover frequency which leads to the following requirement:

$$f_{P2} < f_C$$ (control loop bandwidth requirement)

The following equations calculate phase margin

$$PM = 180° - \tan^{-1}\left(\frac{f_C}{f_{P1}}\right) - \tan^{-1}\left(\frac{f_C}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (general boost mode phase margin)

Assuming $f_{P1} << f_C$, then

$$PM = 90° - \tan^{-1}\left(\frac{f_C}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (simplified boost mode phase margin)

Assuming f_{P1} and f_{P2} are both much lower than crossover frequency, then

$$PM = \tan^{-1}\left(\frac{f_C}{f_{Z1}}\right)$$ (reduced boost mode phase margin)

10 Applying the PS5610

10.1 Prevent Switching Noise from Coupling into the CSP and CSN Pins

When laying out the printed circuit board (PCB) for the PS5610 care should be taken to prevent switching noise from coupling into the CSP and CSN pins. Such coupled switching noise can cause the VSW waveform to become distorted or perhaps even oscillate. Generally R_{CS} should be located close to the CSP and CSN pins. Also, an optional capacitor may be placed in parallel with R_{CS}. However, make sure that the corner frequency of the resulting RC pole is at least a factor of ten above the crossover frequency of the PS5610's control loop.

10.2 V_{CS} Common Mode Considerations

Due to the finite common mode rejection of the CSP/CSN amplifier, the performance of the PS5610 will be negatively impacted by high frequency V_{CS} common mode voltage changes. It is therefore important to decouple the CSP input with a nearby high frequency capacitor. For the buck configuration this can be simply implemented with the VIN capacitor. For the boost and buck-boost configurations it is important to add a high frequency decoupling capacitor between CSP and GND. However, a large capacitor will impact the LED diming performance. Some reduction in common mode voltage deviation can be gained by placing the current sense resistor (R_{CS}) within the LED string to reduce the voltage change at CSP/CSN but still satisfy the "VCSP" spec.

10.3 RGB Lighting Application

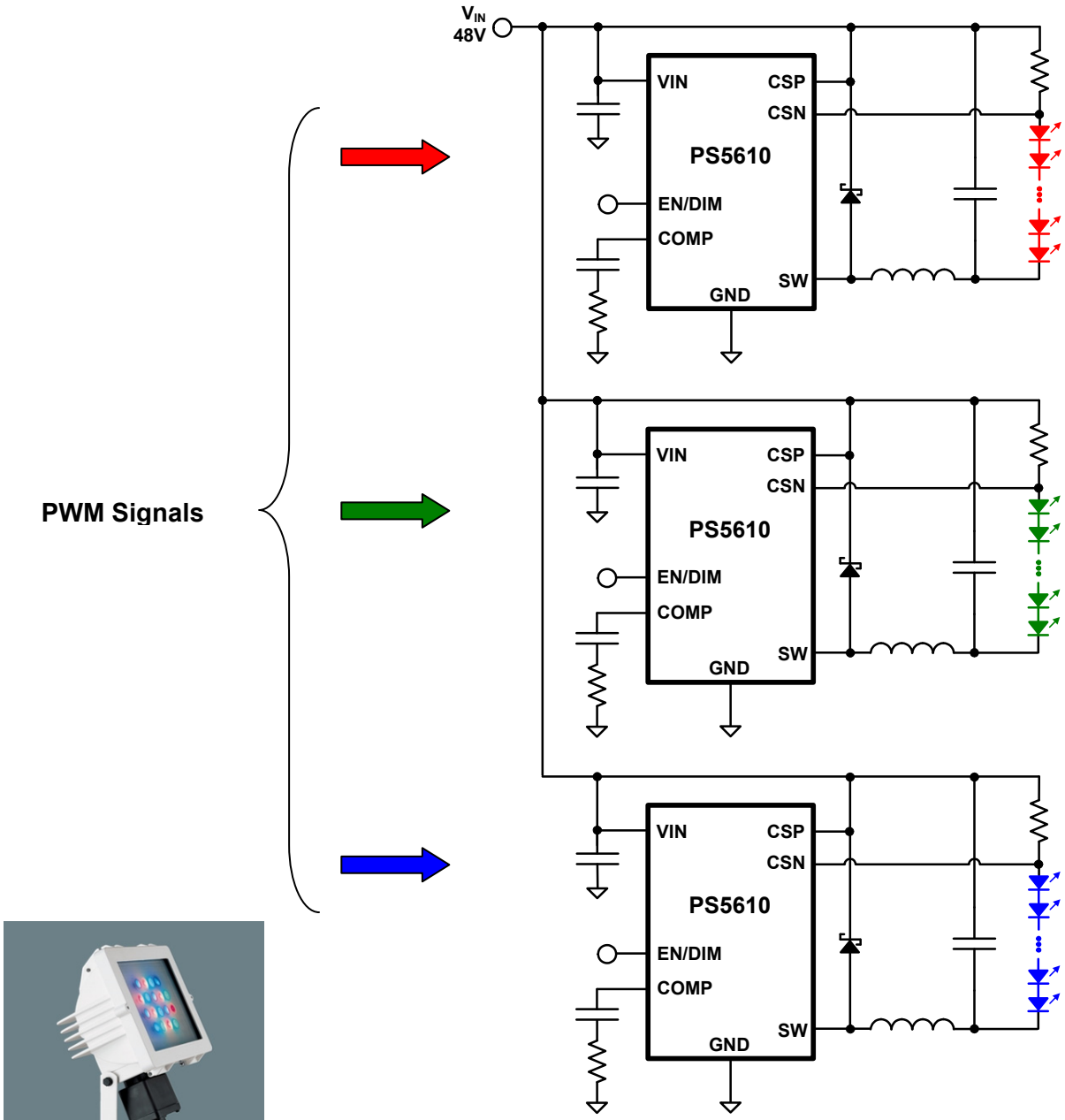


Figure 10.1: Sample Lighting Application

11 Package Mechanical Information

11.1 MLPD (5 mm x 6 mm - Exposed Heat Slug)

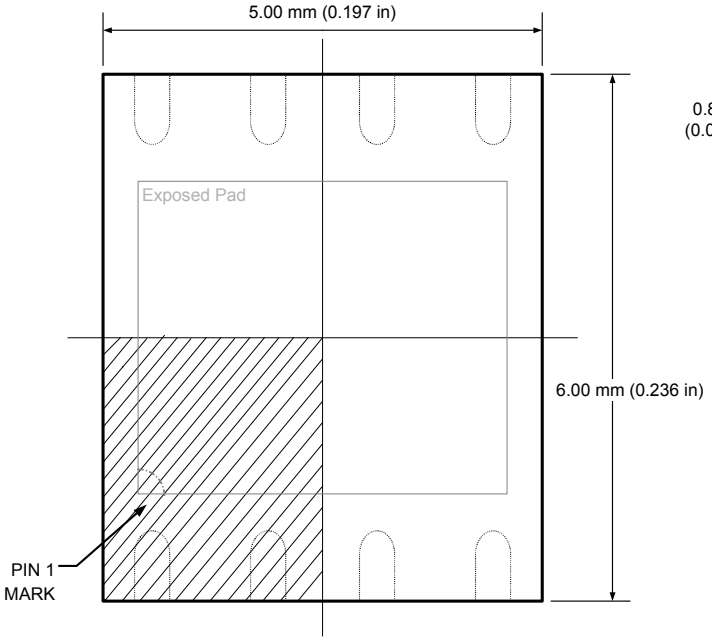


Figure 11.1: Package Top View

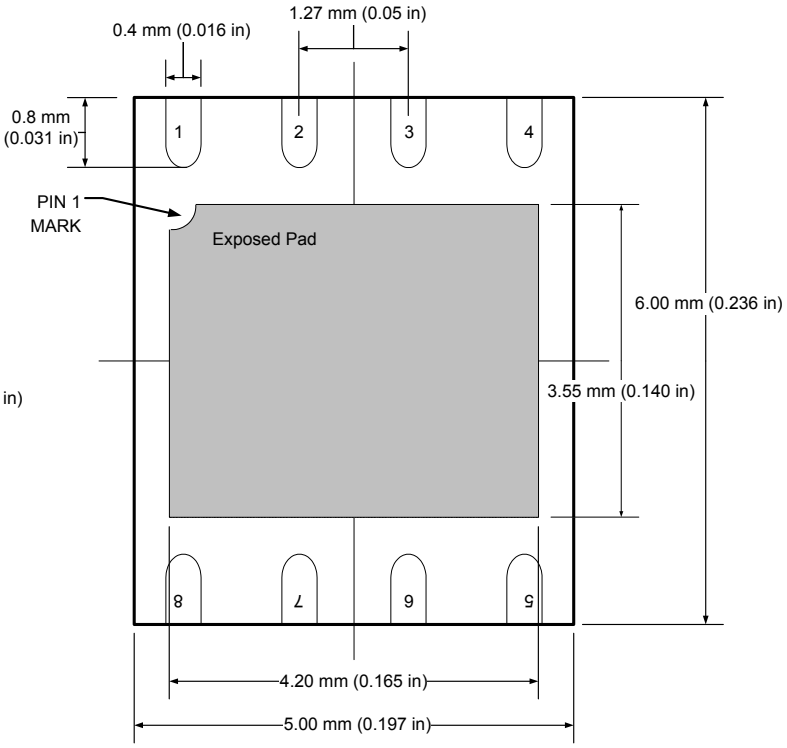


Figure 11.2: Package Bottom View

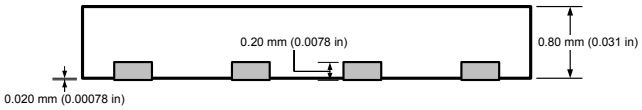


Figure 11.3: Package Side View

NOTE:

- Control dimension is in millimeters. Dimension in bracket is inches.
- Exposed pad; 4.20+/-0.1mm x 3.55 +/- 0.1mm.

11.2 HSOP-8 (Exposed Heat Slug)

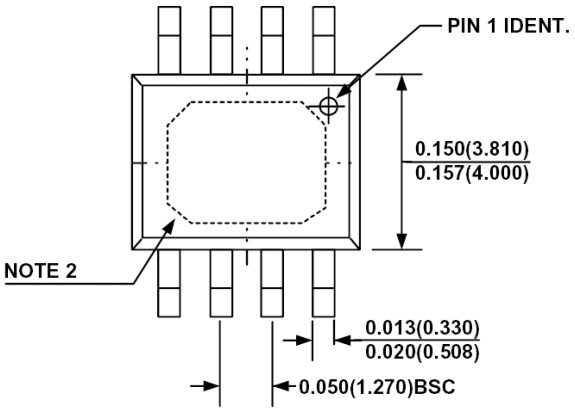


Figure 11.4: Package Top View

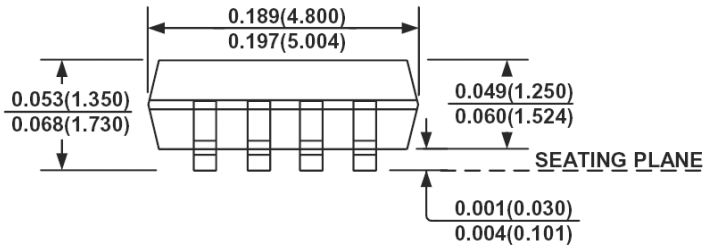


Figure 11.6: Package Side View

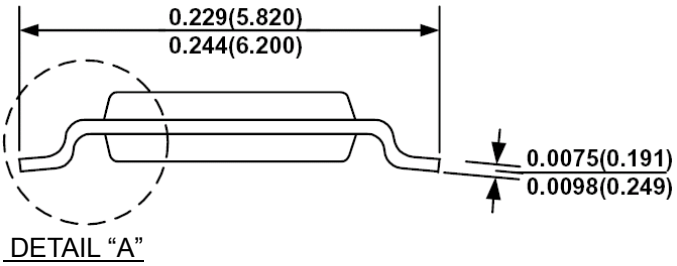
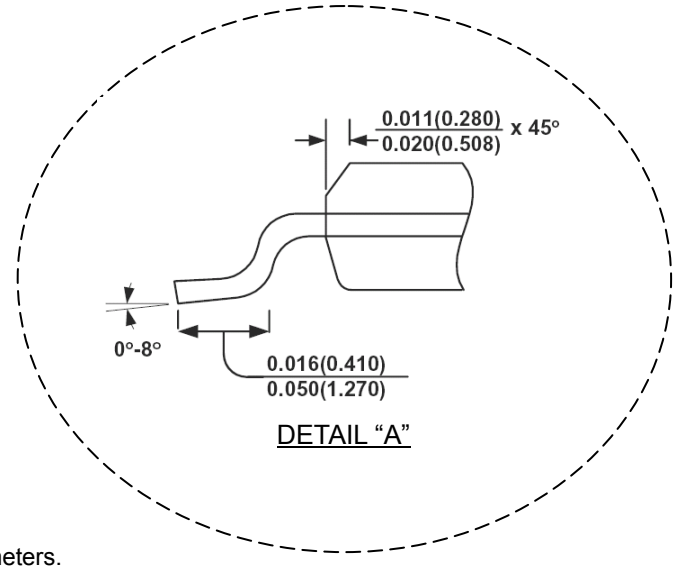


Figure 11.5: Package End View



NOTE:

- Control dimension is in inches. Dimension in bracket is millimeters.
- Exposed pad; 2.55+/-0.25mm x 3.38 +/- 0.44mm.
- Recommended Solder Board Area: 2.80mm x 3.82mm = 10.7mm^2 (16.6mil^2)

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