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LCD MODULE SPECIFICATION

MODEL NO.

BC2004AYPLCU

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

1.General Specification

ITEM	STANDARD VALUE	UNIT
Number of Characters:	20 characters×4 Lines	
Module dimension:	98.0×60.0×13.6(MAX)mm	mm
View area:	77.0×25.2mm	mm
Active area:	70.4×20.8mm	mm
Character size:	(L)2.95×(W)4.75mm	mm
Character pitch:	(L)3.55×(W)5.35mm	mm
LCD type:	STN, positive, transflective Yellow	
Duty:	1/16	
View direction:	6 o'clock	
Backlight:	LED yellow green	

2.Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{OP}	-30	—	+80	℃
Storage Temperature	T_{ST}	-40	—	+85	℃
Input Voltage	V_I	V_{SS}	—	V_{DD}	V
Supply Voltage For Logic	V_{DD}-V_{SS}	-0.3	—	7	V
Supply Voltage For LCD	V_{DD}-V_0	-0.3	—	13	V
Supply current FOR LED B/L	I_{LED}	—	—	420	mA

3.Electrical Characteristics

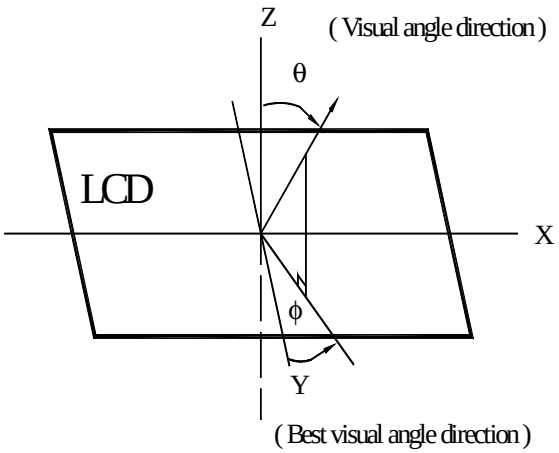
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V_{DD}-V_{SS}	—	4.5	—	5.5	V
Supply Voltage For LCD	V_{DD}-V_0	Ta=-30℃	—	—	—	V
		Ta=25℃	—	4.2	—	V
		Ta=+80℃	—	—	—	V
Input High Vol	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Vol	V_{IL}	—	—	—	0.6	V
Output High Vol	V_{OH}	—	2.4	—	—	V
Output Low Vol.	V_{OL}	—	—	—	0.4	V
Supply Current	I_{DD}	V_{DD}=5V	—	1.6	—	mA

4.Optical Characteristics

ITEM	SYMBAL	CONDITION	MIN.	TYP.	MAX.	UNIT
View Angle	(V) θ	CR≧2	10		40	deg
	(H) φ	CR≧2	-30		30	deg
Contrast Ratio	CR	—		5		—
Response Time	T rise	—		200	300	ms
	T fall	—		200	300	ms

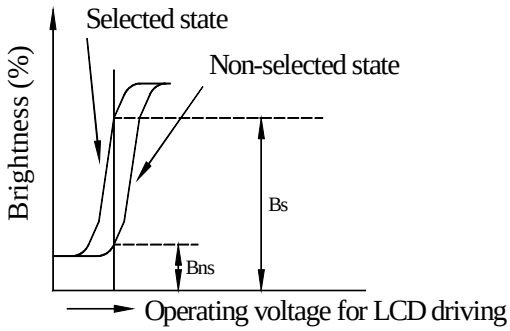
4.1 Definitions

■View Angles

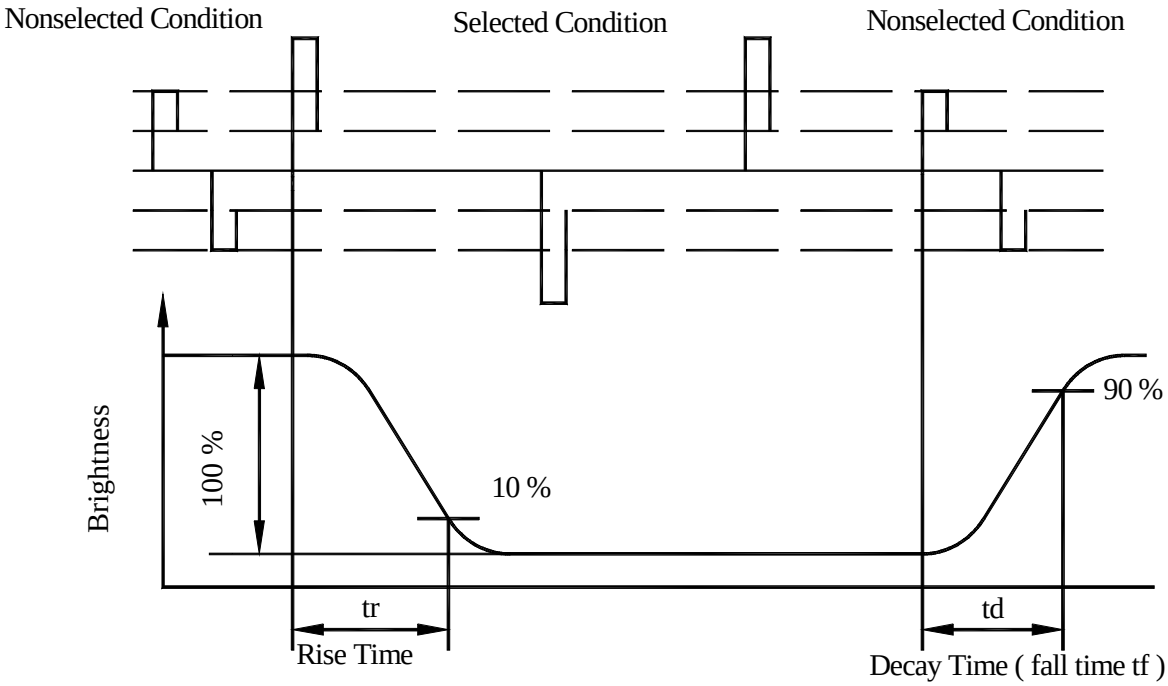


■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



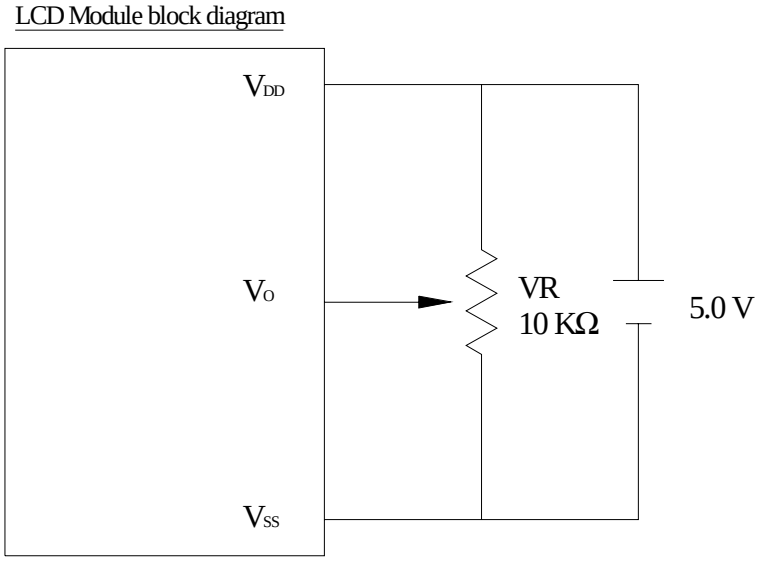
■Response Time



5.Interface Pin Function

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H:DATA, L:Instruction code
5	R/W	H/L	H:Read(MPU→Module)L:Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	—	Power supply for LED backlight (+)
16	K	—	Power supply for LED backlight (-)

6.Power Supply for LCD Module and Contrast Adjust



VDD-V0:LCD Operating Voltage

7.Backlight Information

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	—	280		mA	V=4.2V
Supply Voltage	V	—	4.2	4.6	V	
Reverse Voltage	VR	—	—	8	V	
Luminous Intensity	IV	60	—	—	CD/M^2	ILED=280mA
Wave Length	λ p		574		nm	ILED=280mA
Life Time		—	100000	—	Hr.	V≦4.6V
Color	Yellow Green					

8.Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

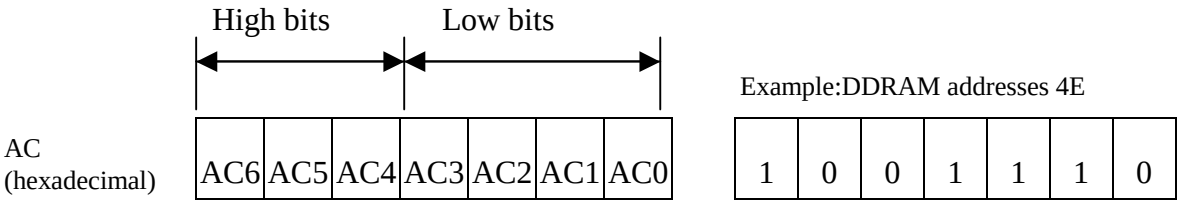
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

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For 5 * 8 dot character patterns

Character Codes (DDRAM data)	CGRAM Address		Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low		7 6 5 4 3 2 1 0 High Low
0 0 0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * ■ ■ ■ ■ 0 * * * ■ 0 0 0 ■ * * * ■ 0 0 0 ■ * * * ■ ■ ■ ■ 0 * * * ■ 0 ■ 0 0 * * * ■ 0 0 ■ 0 * * * ■ 0 0 0 ■ * * * 0 0 0 0 0
0 0 0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * ■ 0 0 0 ■ * * * 0 ■ 0 ■ 0 * * * ■ ■ ■ ■ ■ * * * 0 0 ■ 0 0 * * * ■ ■ ■ ■ ■ * * * 0 0 ■ 0 0 * * * 0 0 ■ 0 0 * * * 0 0 0 0 0
		0 0 0 0 0 1	* * *
0 0 0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1	* * *

Character pattern(1)

Cursor pattern

Character pattern(2)

Cursor pattern

For 5 * 10 dot character patterns

Character Codes (DDRAM data)	CGRAM Address		Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low		7 6 5 4 3 2 1 0 High Low
0 0 0 0 * 0 0 0	0 0	0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0	* * * 0 0 0 0 0 * * * 0 0 0 0 0 * * * ■ 0 ■ ■ 0 * * * ■ ■ 0 0 ■ * * * ■ 0 0 0 ■ * * * ■ 0 0 0 ■ * * * ■ ■ ■ ■ 0 * * * ■ 0 0 0 0 * * * ■ 0 0 0 0 * * * ■ 0 0 0 0 * * * 0 0 0 0 0
		1 1 1 1	* * * * * * * * *

Character pattern

Cursor pattern

■ : " High "

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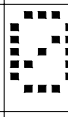
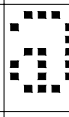
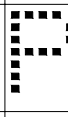
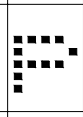
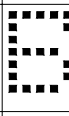
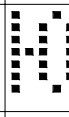
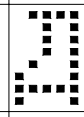
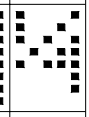
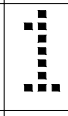
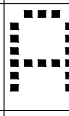
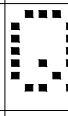
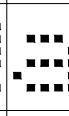
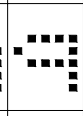
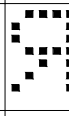
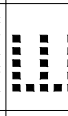
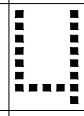
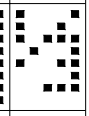
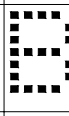
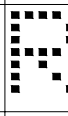
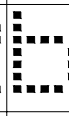
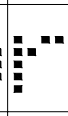
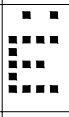
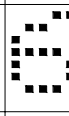
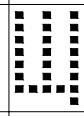
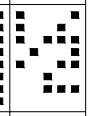
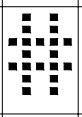
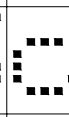
Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

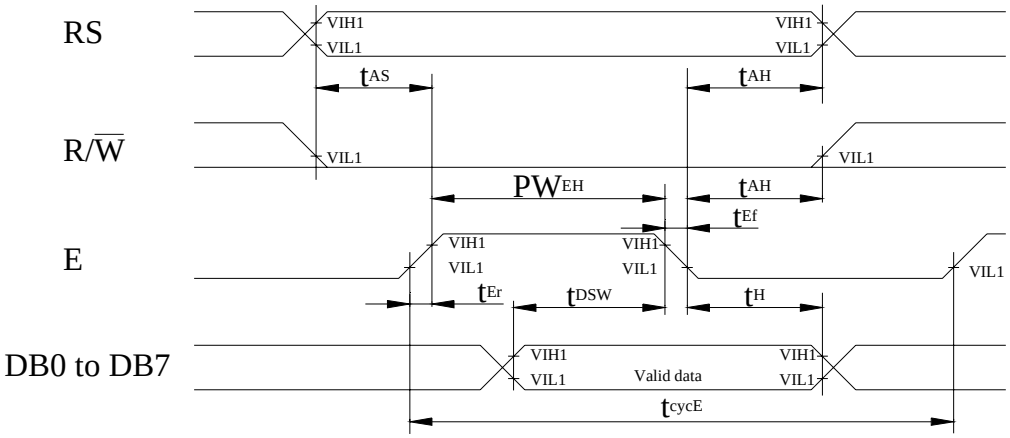
9.Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “00H” to DDRAM and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

＊ ”—”：don’t care

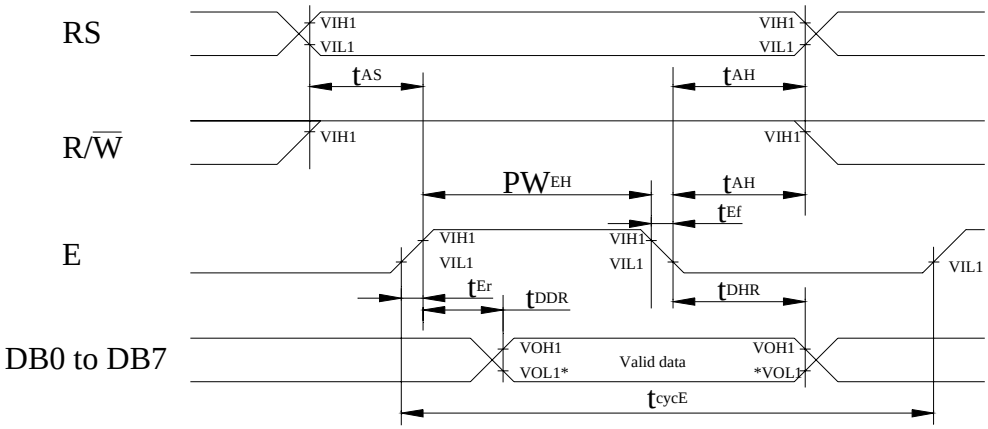
10.Timing Characteristics

10.1 Write Operation



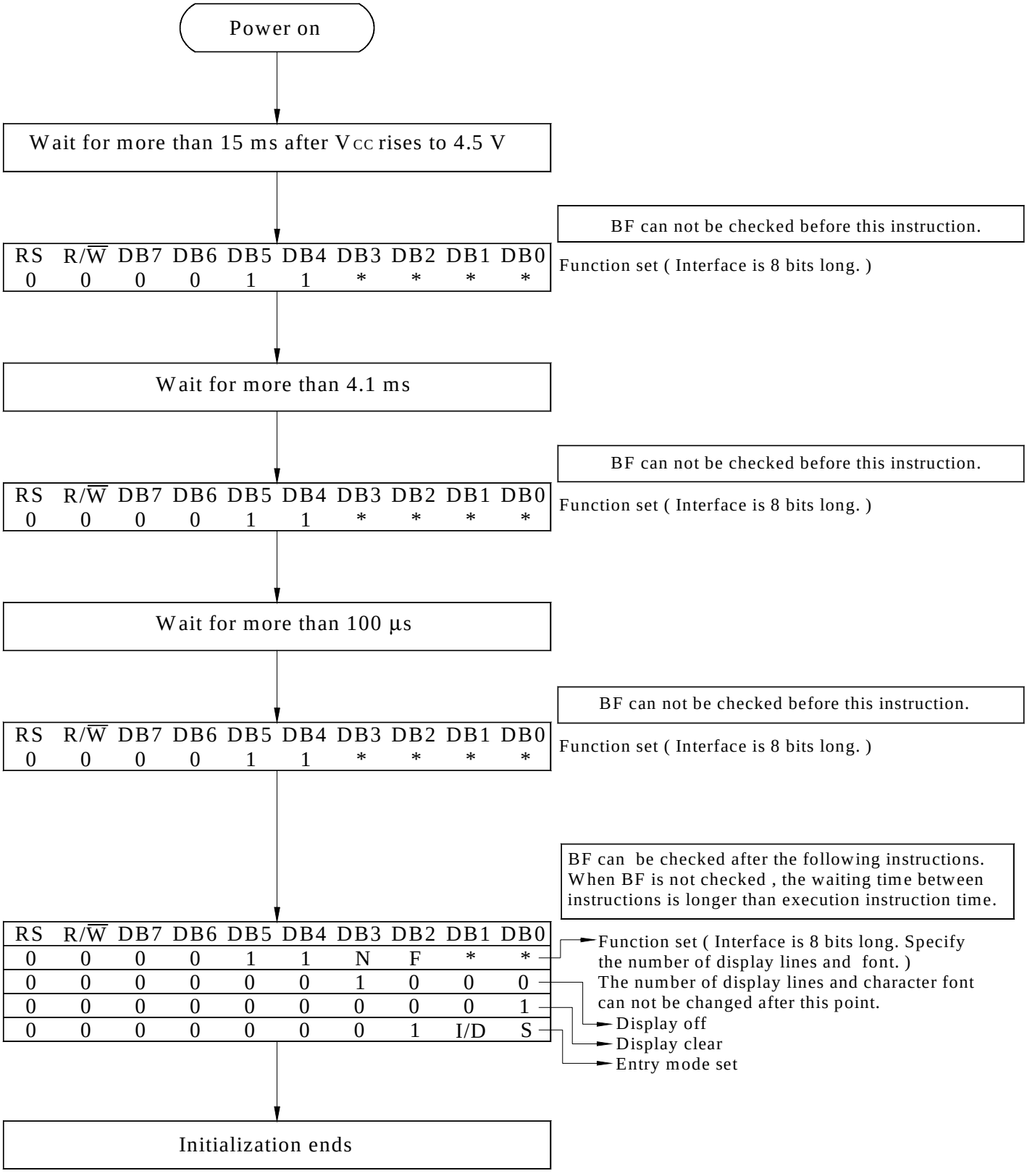
Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data set-up time	t_{DSW}	80	—	—	ns
Data hold time	t_{H}	10	—	—	ns

10.2 Read Operation

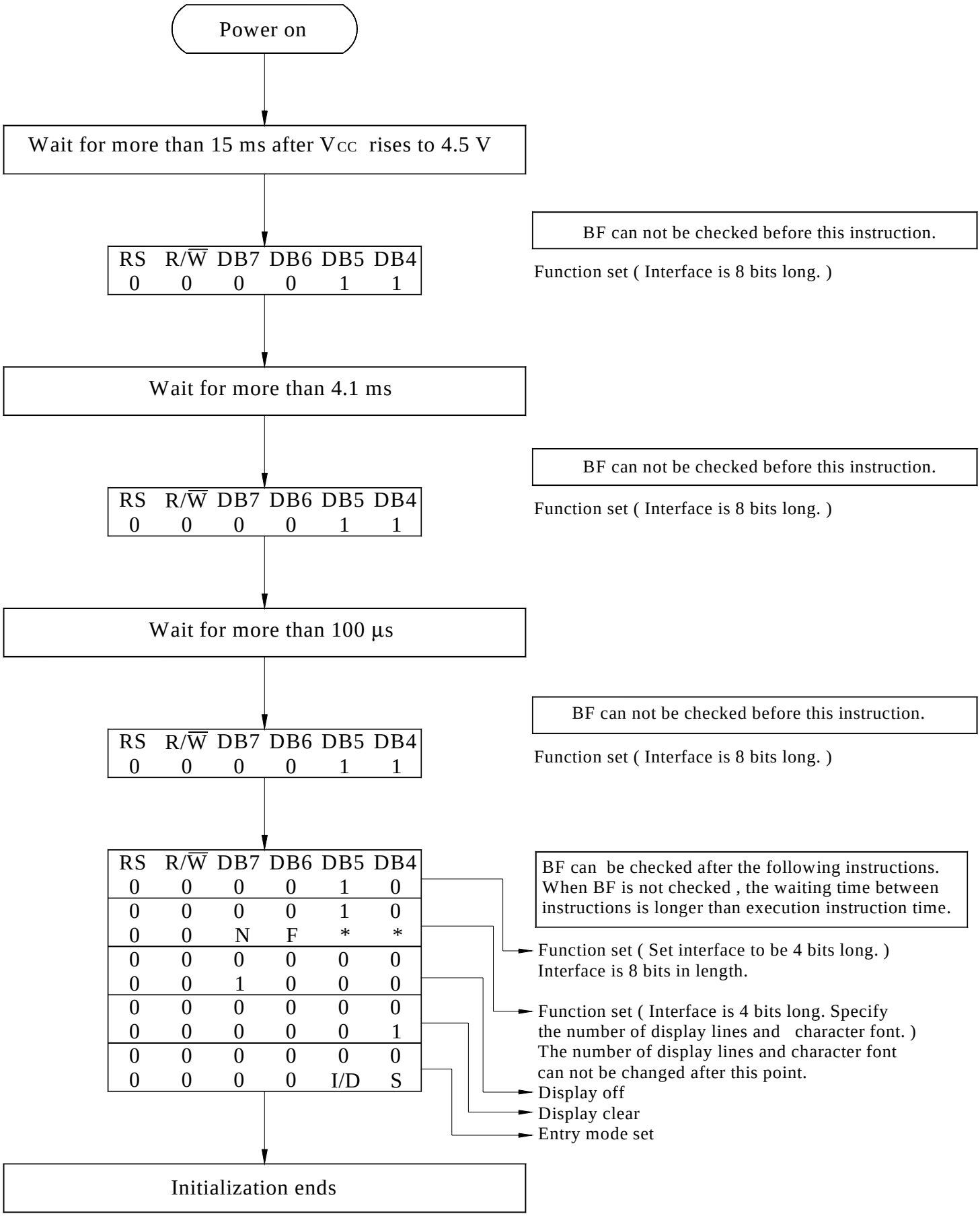


NOTE: *VOL1 is assumed to be 0.8V at 2 MHZ operation.

ITEM	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data delay time	t_{DDR}	—	—	160	ns
Data hold time	t_{DHR}	5	—	—	ns



8-Bit Ineterface



4-Bit Ineterface

11.Quality Assurance

◆ Screen Cosmetic Criteria

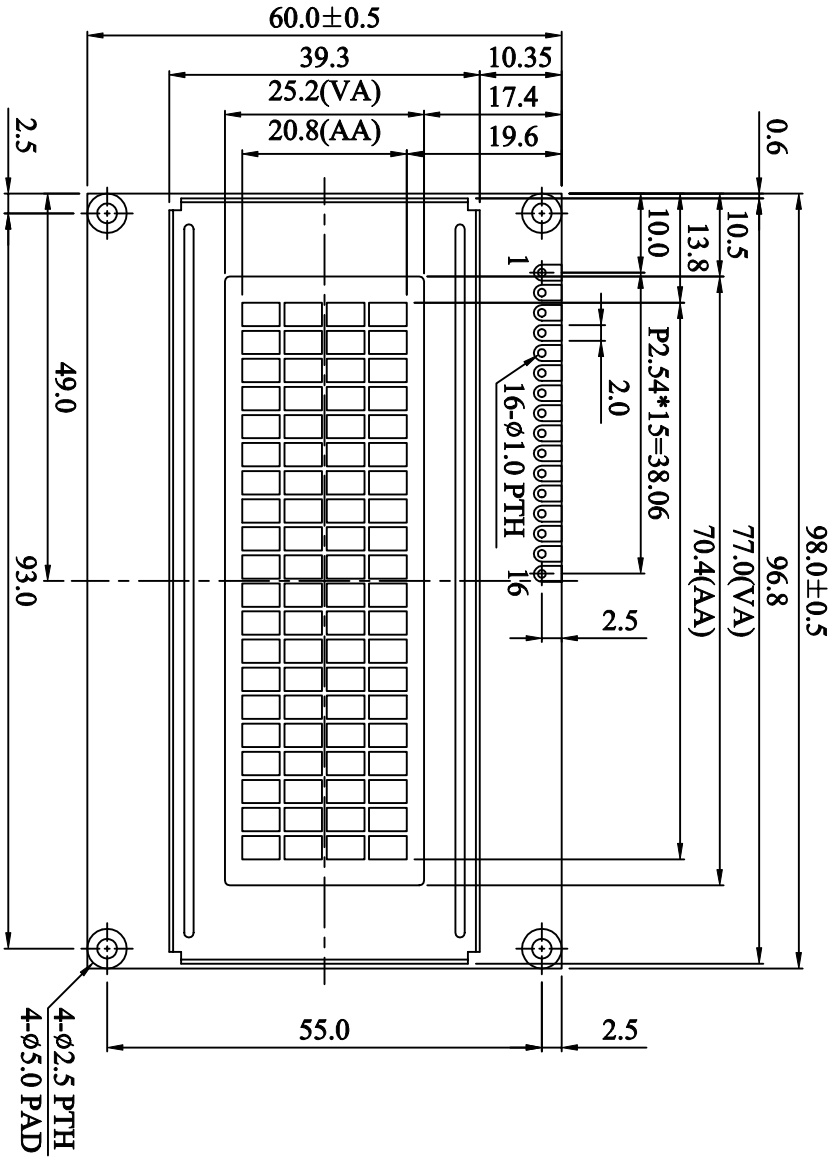
No.	Defect	Judgement Criterion	Partition
1	Spots	A)Clear Size:d mm — Acceptable Qty in active area d ≦0.1 — Disregard 0.1<d≦0.2 — 6 0.2<d≦0.3 — 2 0.3<d — 0 Note:Including pin holes and defective dots which must be within one pixel size. B)Unclear Size:d mm — Acceptable Qty in active area d ≦0.2 — Disregard 0.2<d≦0.5 — 6 0.5<d≦0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarizer	Size:d mm — Acceptable Qty in active area d≦0.3 — Disregard 0.3<d≦1.0 — 3 1.0<d≦1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

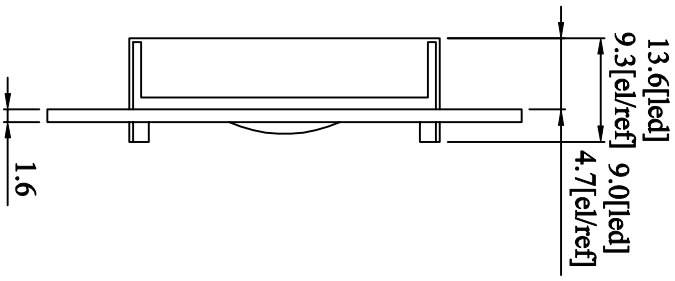
12.RELIABILITY

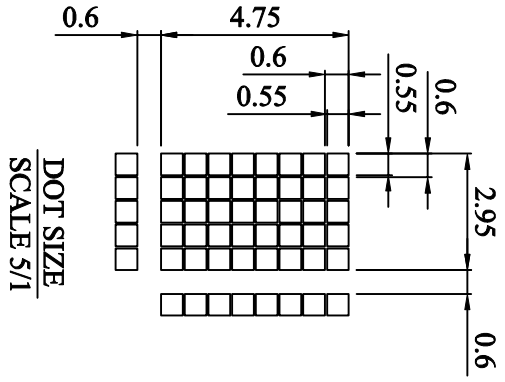
■Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 200hrs	——
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-20℃ 200hrs	——
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	——
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	——
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 96hrs	——
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40℃,90%RH 96hrs	——
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -20℃ 25℃ 60℃ ◄——————► 30min 5min 30min 1 cycle	-20℃/60℃ 10 cycles	——
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃


60.0±0.5
39.3
10.35
25.2(VA)
17.4
20.8(AA)
19.6
2.5
0.6
10.0
13.8
10.5
1
P2.54*15=38.06
2.0
16-ø1.0 PTH
49.0
93.0
16
2.5
70.4(AA)
77.0(VA)
96.8
98.0±0.5
4-ø2.5 PTH
4-ø5.0 PAD
55.0
2.5


13.6[led]
9.3[el/ref]
9.0[led]
4.7[el/ref]
1.6


0.6
4.75
0.6
0.55
0.55
0.6
DOT SIZE
SCALE 5/1
2.95
0.6