TINSHARP Industrial Co., Ltd.

DATA SHEET

LCM MODULE

TG12864-COG7D

Specification for Approval

APPROVED BY	CHECKED BY	PREPARED BY

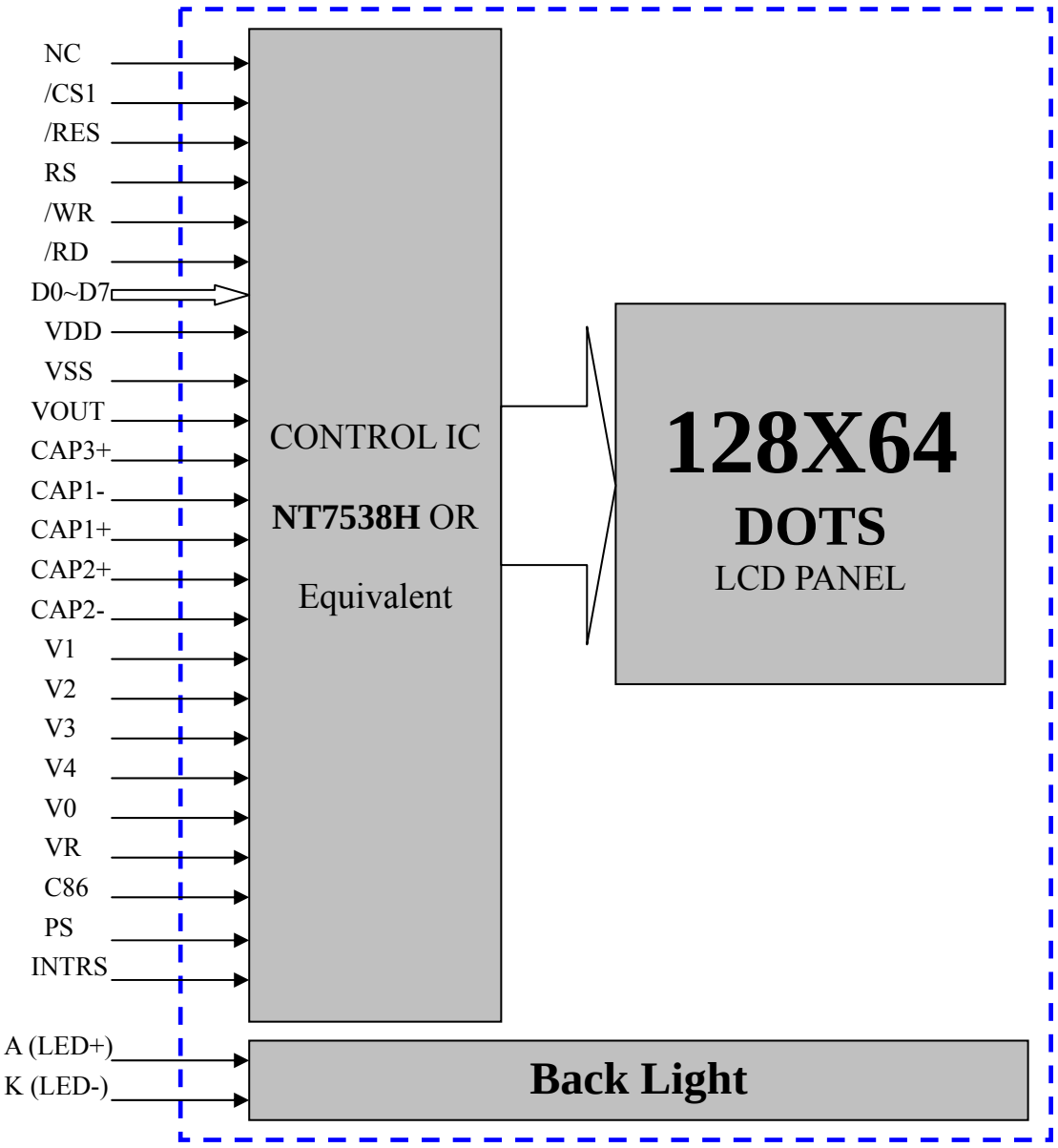
ISSUED: V00 2013-11-26

CONTENTS

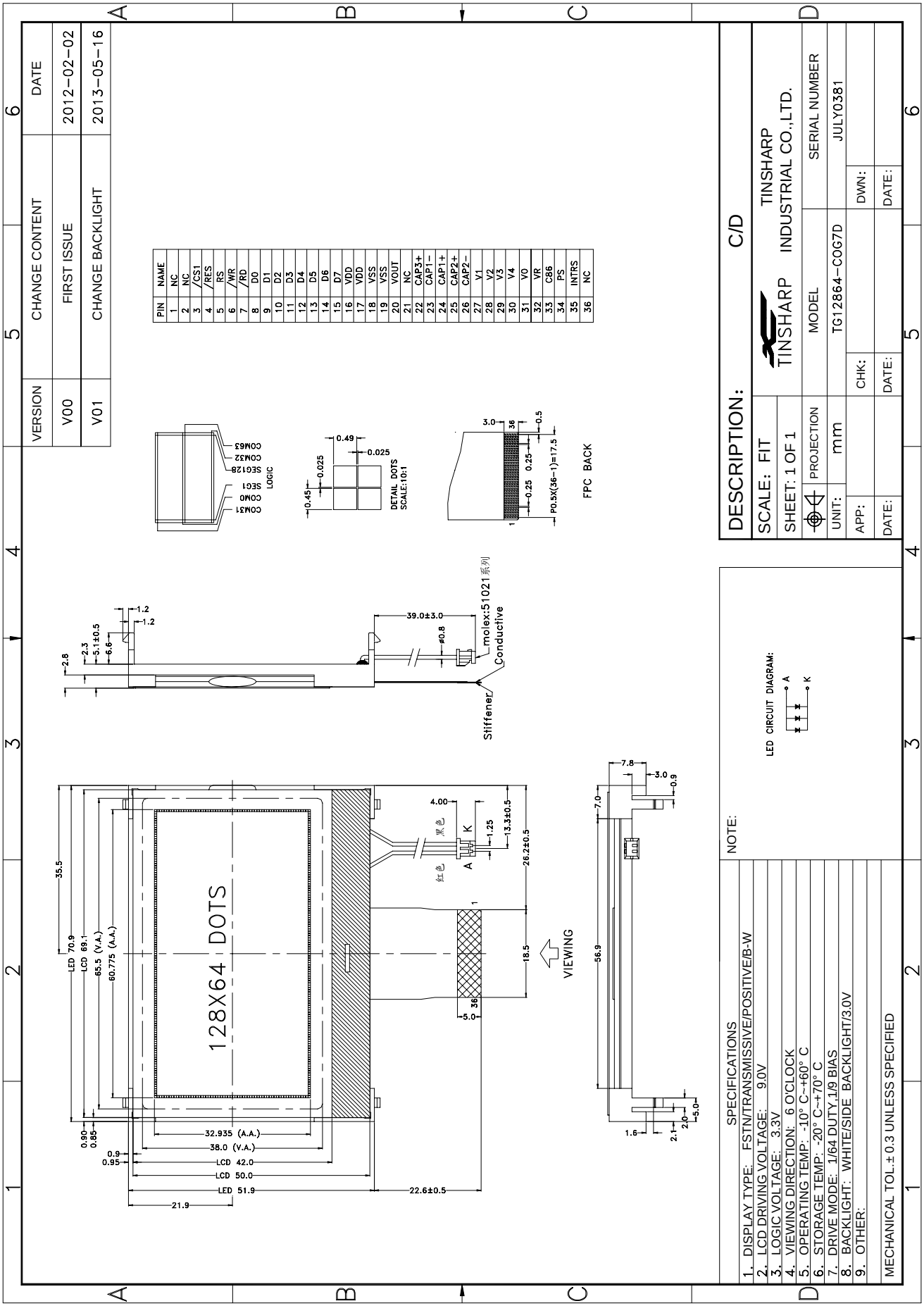
FUNCTIONS & FEATURES

- Construction : COG (Chip-on-Glass)
- Display Format : 128x64 dots
- Display Type : FSTN, Transmissive, Positive, B-W
- Controller : NT7538H or equivalent controller
- Interface : 8-bit parallel interface
- Backlight : White/side light
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65 Duty Cycle, 1/9 Bias
- Power Supply Voltage : 3.3 V
- V_{LCD} Adjustable For Best Contrast : 9.0 V ($V_{OP.}$)
- Operation temperature : -10℃ to +60℃
- Storage temperature : -20℃ to +70℃

BLOCK DIAGRAM



MODULE OUTLINE DRAWING:



INTERFACE PIN FUNCTIONS:

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>--</td><td>Non-connection.</td></tr>
<tr><td>2</td><td>NC</td><td>--</td><td>Non-connection.</td></tr>
<tr><td>3</td><td>/CS1</td><td>H/L</td><td>This is the chip select signal. When /CS1=”L”, then the chip select becomes active, and data /command I/O is enable.</td></tr>
<tr><td>4</td><td>/RES</td><td>H/L</td><td>When /RES is set to “L”, the settings are initialized.</td></tr>
<tr><td>5</td><td>RS</td><td>H/L</td><td>This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.
RS=L: D0 to D7 are control data.
RS=H: D0 to D7 are display data.</td></tr>
<tr><td>6</td><td>/WR</td><td>H/L</td><td>When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal.
When connected to a 6800 Series MPU, this is the read/write control signal input terminal.
When R/W = “H”: Read
When R/W = “L”: Write</td></tr>
<tr><td>7</td><td>/RD</td><td>H/L</td><td>When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the NT7538 data bus is in an output status when this signal is “L”.
When connected to a 6800 Series MPU, this is active HIGH.
This is used as an enable clock input of the 6800 series MPU.</td></tr>
<tr><td>8</td><td>D0</td><td>H/L</td><td rowspan="8">This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S=“L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). When the serial interface is selected, fix D0~D5 pads to VDD or VSS level.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
<tr><td>9</td><td>D1</td><td>H/L</td></tr>
<tr><td>10</td><td>D2</td><td>H/L</td></tr>
<tr><td>11</td><td>D3</td><td>H/L</td></tr>
<tr><td>12</td><td>D4</td><td>H/L</td></tr>
<tr><td>13</td><td>D5</td><td>H/L</td></tr>
<tr><td>14</td><td>D6</td><td>H/L</td></tr>
<tr><td>15</td><td>D7</td><td>H/L</td></tr>
<tr><td>16-17</td><td>VDD</td><td>+3.3V</td><td>Supply voltage for logic operating.</td></tr>
<tr><td>18-19</td><td>VSS</td><td>0V</td><td>Ground output for pad option.</td></tr>
<tr><td>20</td><td>VOUT</td><td>--</td><td>DC/DC voltage converter output.</td></tr>
<tr><td>21</td><td>NC</td><td>--</td><td>NC</td></tr>
<tr><td>22</td><td>CAP3+</td><td>H/L</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the C1- terminal.</td></tr>
<tr><td>23</td><td>CAP1-</td><td>H/L</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the C1+ terminal.</td></tr>
<tr><td>24</td><td>CAP1+</td><td>H/L</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the C1- terminal.</td></tr>
<tr><td>25</td><td>CAP2+</td><td>H/L</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the C2- terminal.</td></tr>
<tr><td>26</td><td>CAP2-</td><td>H/L</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the C2+ terminal.</td></tr>
<tr><td>27</td><td>V1</td><td>H/L</td><td rowspan="5">LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship: V0≥V1≥V2≥V3≥V4≥VSS2.
When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD bias SET command.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/4 bias</td><td>3/4 V0</td><td>2/4 V0</td><td>2/4 V0</td><td>1/4 V0</td></tr>
<tr><td>1/5 bias</td><td>4/5 V0</td><td>3/5 V0</td><td>2/5 V0</td><td>1/5 V0</td></tr>
<tr><td>1/6 bias</td><td>5/6 V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 bias</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 bias</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 bias</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>28</td><td>V2</td><td>H/L</td></tr>
<tr><td>29</td><td>V3</td><td>H/L</td></tr>
<tr><td>30</td><td>V4</td><td>H/L</td></tr>
<tr><td>31</td><td>V0</td><td>H/L</td></tr>
<tr><td>32</td><td>VR</td><td>--</td><td>Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.</td></tr>
<tr><td>33</td><td>C86</td><td>H/L</td><td>This is the MPU interface switch terminal
C86 = “H”: 6800 Series MPU interface
C86 = “L”: 8080 Series MPU interface</td></tr>
<tr><td>34</td><td>PS</td><td>H/L</td><td>This is the parallel data input/serial data input switch terminal
P/S = “H”: Parallel data input
P/S = “L”: Serial data input
The following applies depending on the P/S status:
<table>
<tr><td>P/S</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, fix D0~D5 pads to VDD or VSS level. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.</td></tr>
</table>

Pin No.	Symbol	Level	Description
35	INTRS	H/L	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H", Use the internal resistors IRS = "L", Do not use the internal resistors The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.
36	NC	--	Non-connection.

Pin No.	Symbol	Level	Description
1	A (LED+)	+3.0V	Power supply for Back Light.
2	K (LED-)	0V	Ground for Back Light.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃):

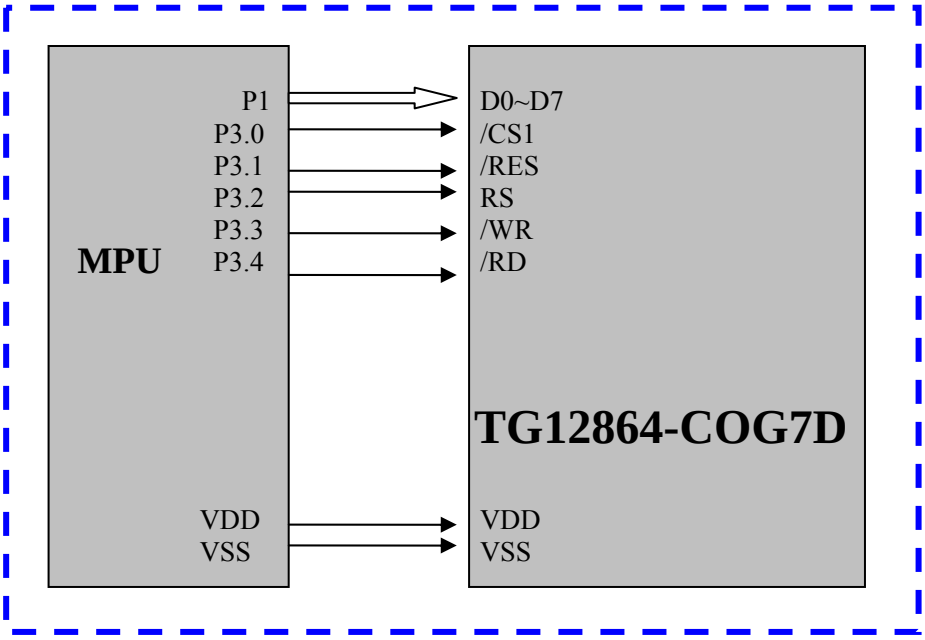
Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	V_{DD}	-0.3	+4.0	V
Supply voltage for LCD	V_o	-0.3	+15.0	V
Input voltage	V_I	-0.3	V_{DD} +0.3	V
Normal Operating temperature	T_{OP}	-10	+60	℃
Normal Storage temperature	T_{ST}	-20	+70	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	T_{YP}	Max	Unit
Supply voltage for logic	VDD	--	2.8	3.3	3.4	V
Supply current for logic	IDD	--	--	2	5	mA
Operating voltage for LCD	VLCD	-10℃				
		+25℃	8.7	9.0	9.3	V
		+60℃				
Input voltage "H" level	VIH	--	0.8 VDD	--	VDD	V
Input voltage "L" level	VIL	--	0	--	0.2VDD	V
Supply voltage for Back Light	VBL	--	2.8	3.0	3.2	V
Supply current for Back Light	IBL	--	35	45	55	mA

CONNECTION WITH MCU

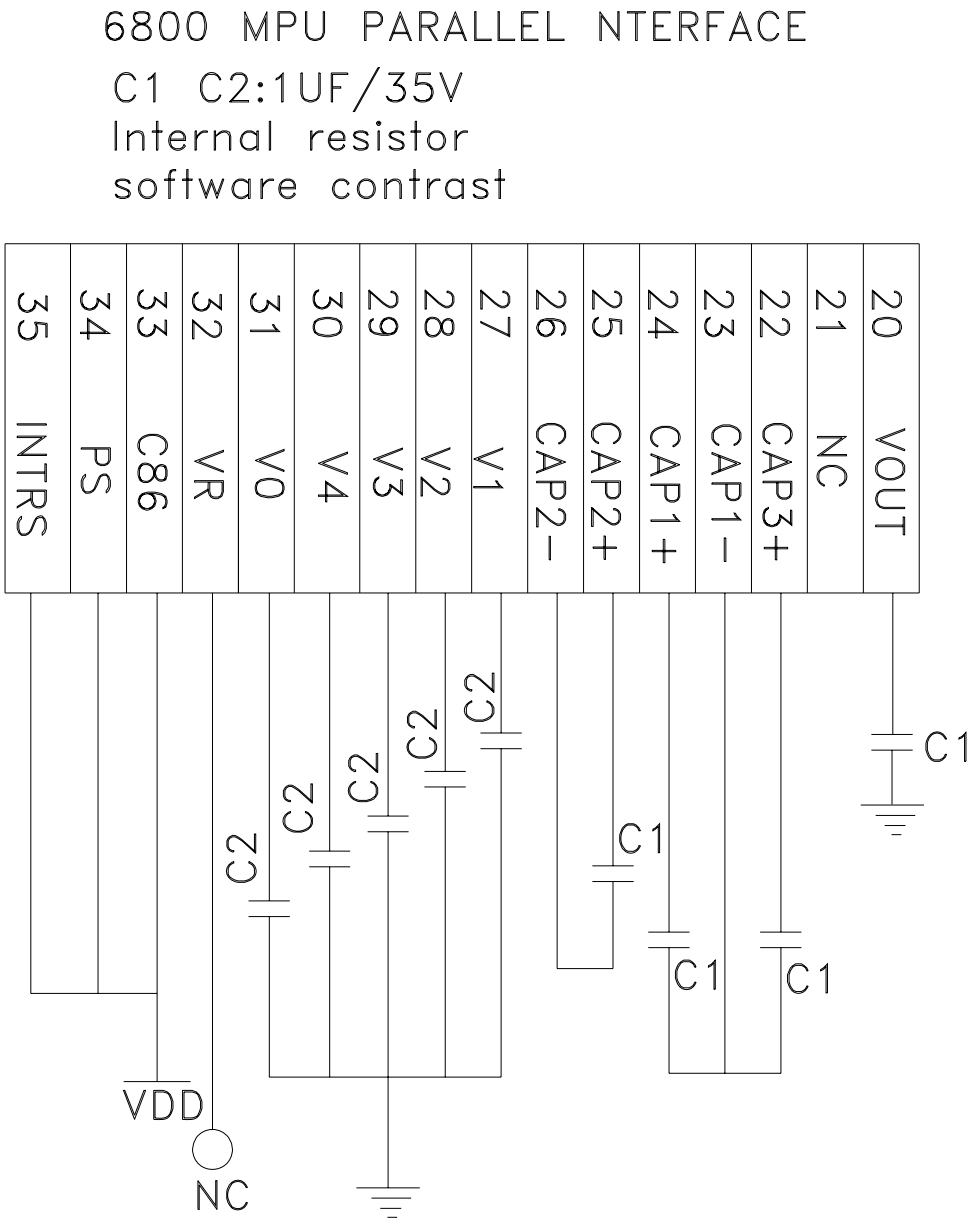


- **NOTES:** parallel interface 8080 Series MPU
  PS= "H"
  INTRS= "H"
  C86= "L"

  parallel interface 6800 Series MPU
  PS= "H"
  INTRS= "H"
  C86= "H"

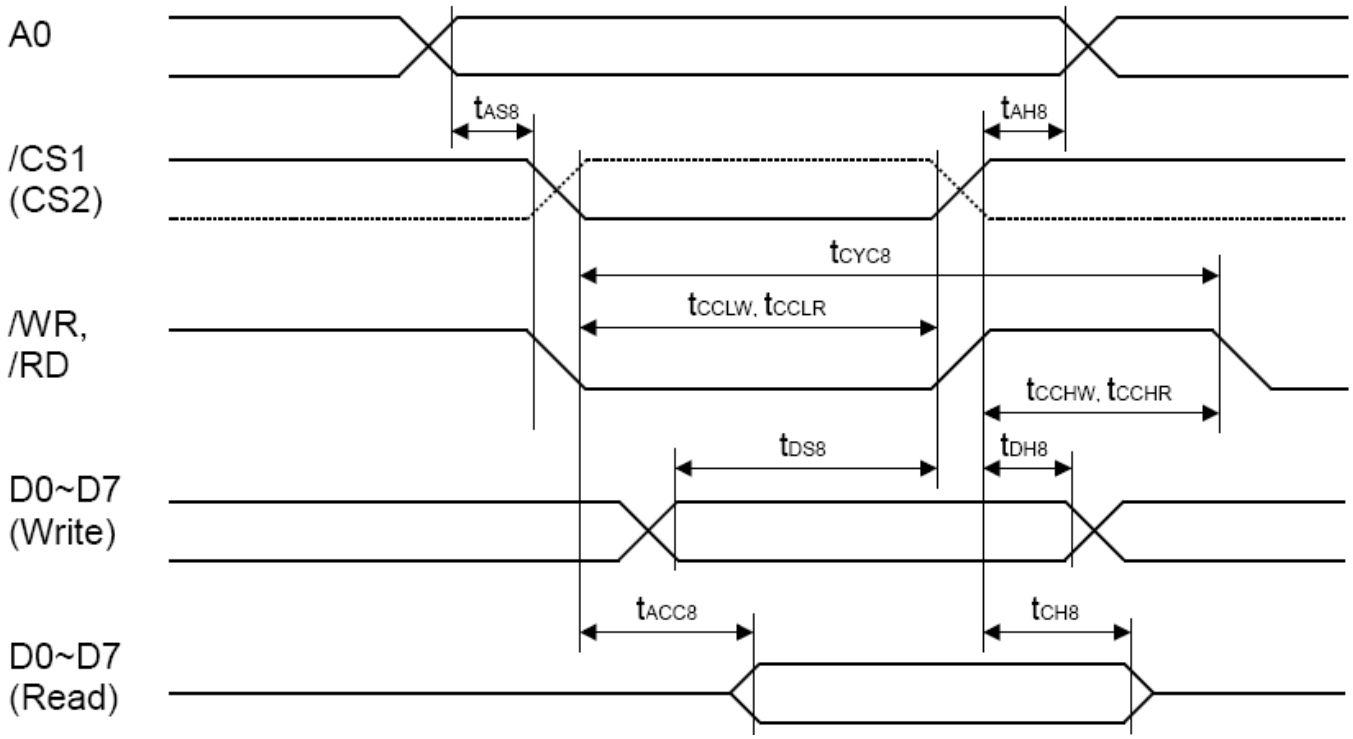
  Serial Interface PS= "L"
  INTRS= "H"
  C86= "H"

Reference Power Supply Circuit for Driving LCD Panel



TIMING CHARACTERISTICS

1. System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

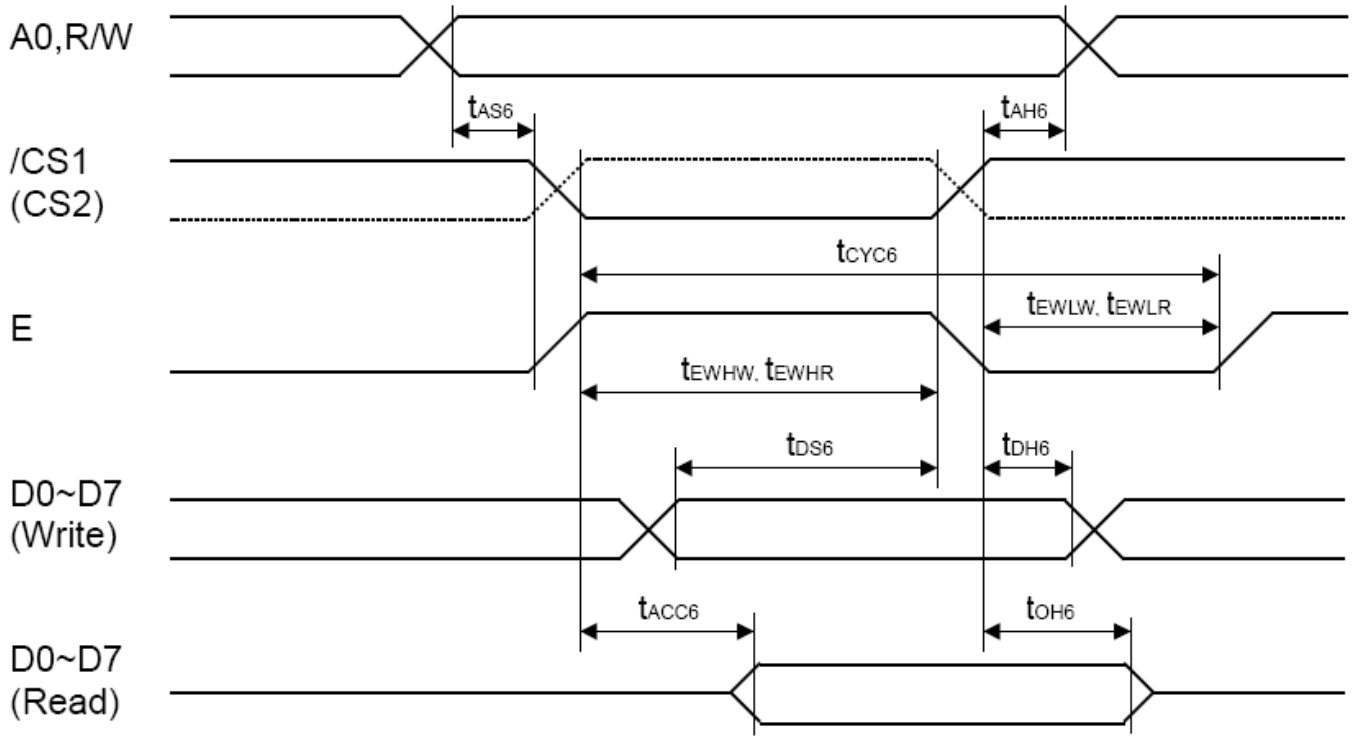
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T_{DS8}	Data setup time	40	-	-	ns	D0~D7
T_{DH8}	Data hold time	0	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{CH8}	Output disable time	5	-	50	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for write, ($t_r + t_f$) < ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) for read.

*2. All timing is specified using 20% and 80% of VDD as the reference.

*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)

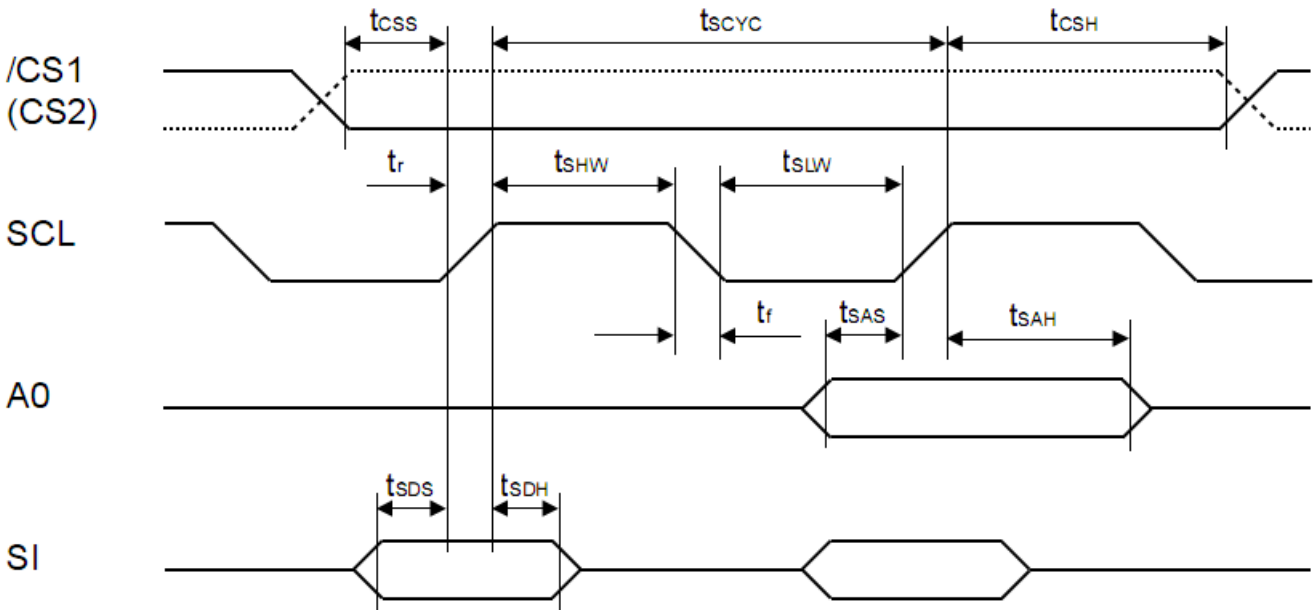


(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0, R/W
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	240	-	-	ns	
t_{EWHW}	Control high pulse width (write)	90	-	-	ns	E
t_{EWHR}	Control high pulse width (read)	120	-	-	ns	E
t_{EWLW}	Control low pulse width (write)	100	-	-	ns	E
t_{EWLR}	Control low pulse width (read)	60	-	-	ns	E
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	0	-	-	ns	
t_{ACC6}	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t_{OH6}	Output disable time	5	-	50	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for write, ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{EWHW} and t_{EWHR} are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

3.Serial Interface Timing:

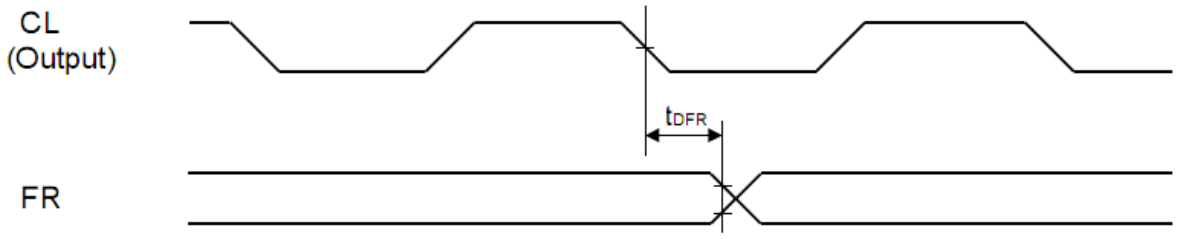


(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	120	-	-	ns	SCL
tSHW	Serial clock H pulse width	60	-	-	ns	SCL
tSLW	Serial clock L pulse width	60	-	-	ns	SCL
tSAS	Address setup time	30	-	-	ns	A0
tSAH	Address hold time	20	-	-	ns	A0
tSDS	Data setup time	30	-	-	ns	SI
tSDH	Data hold time	20	-	-	ns	SI
tCSS	Chip select setup time	20	-	-	ns	/CS1, CS2
tCSH	Chip select hold time	40	-	-	ns	/CS1, CS2

*1. The input signal rise time and fall time (t_r, t_f) is specified as 15ns or less.
*2. All timing is specified using 20% and 80% of VDD as the standard.

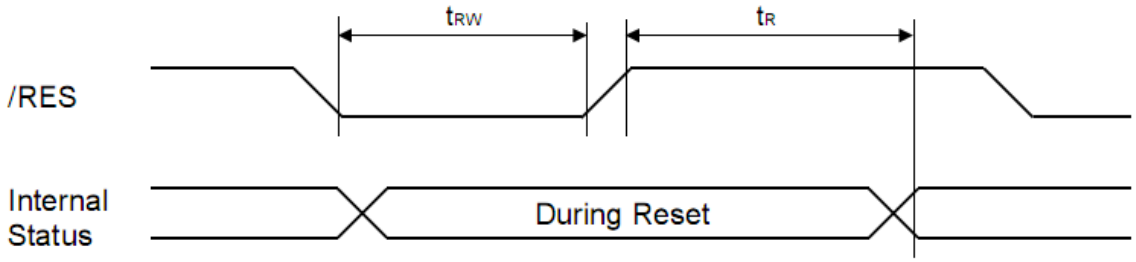
Display Control Timing:



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	20	80	ns	CL = 50 pF

Reset Timing



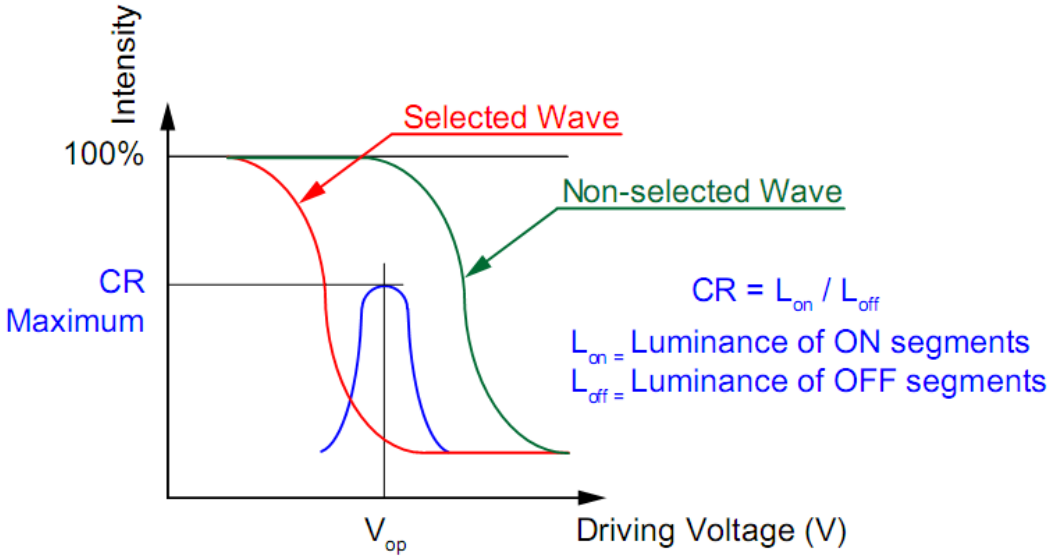
(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	10	-	-	μs	/RES

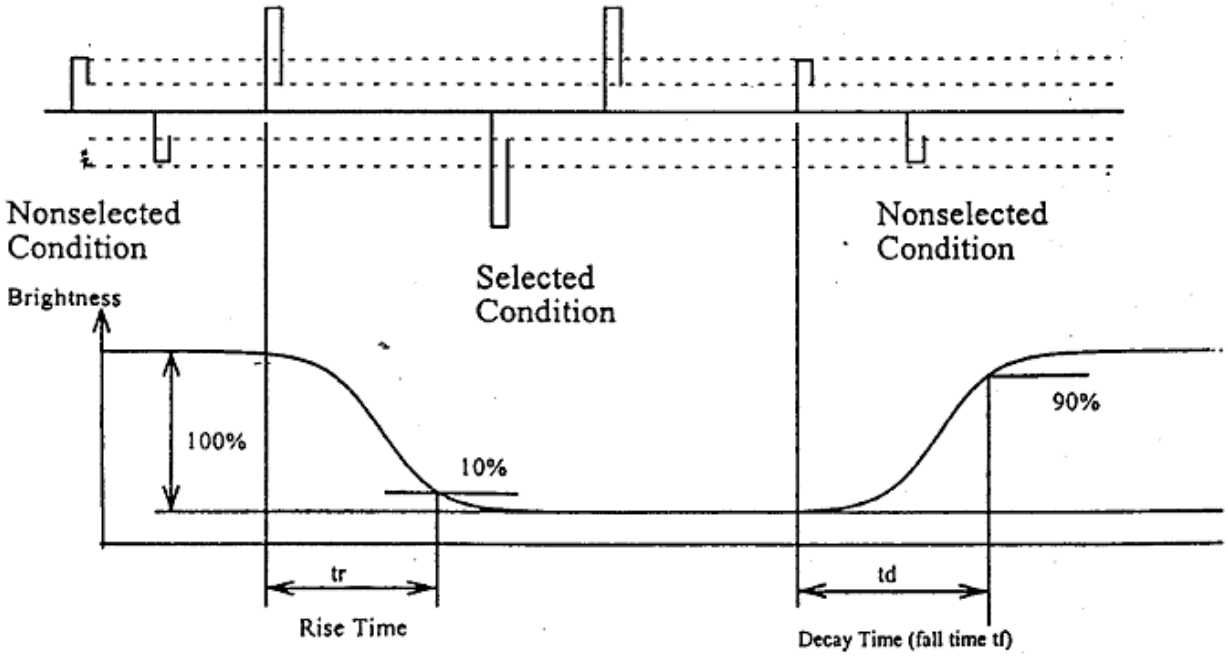
OPTICAL CHARACTERISTICS:

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Contrast ratio	CR	θ=0，Φ=0	-	5	-		
Response time(rise)	Tr	25℃		-	250	ms	
Response time(fall)	Td			-	350		
Viewing angle	θf	25℃					
	θb						
	θl			-		deg.	
	θr			-			

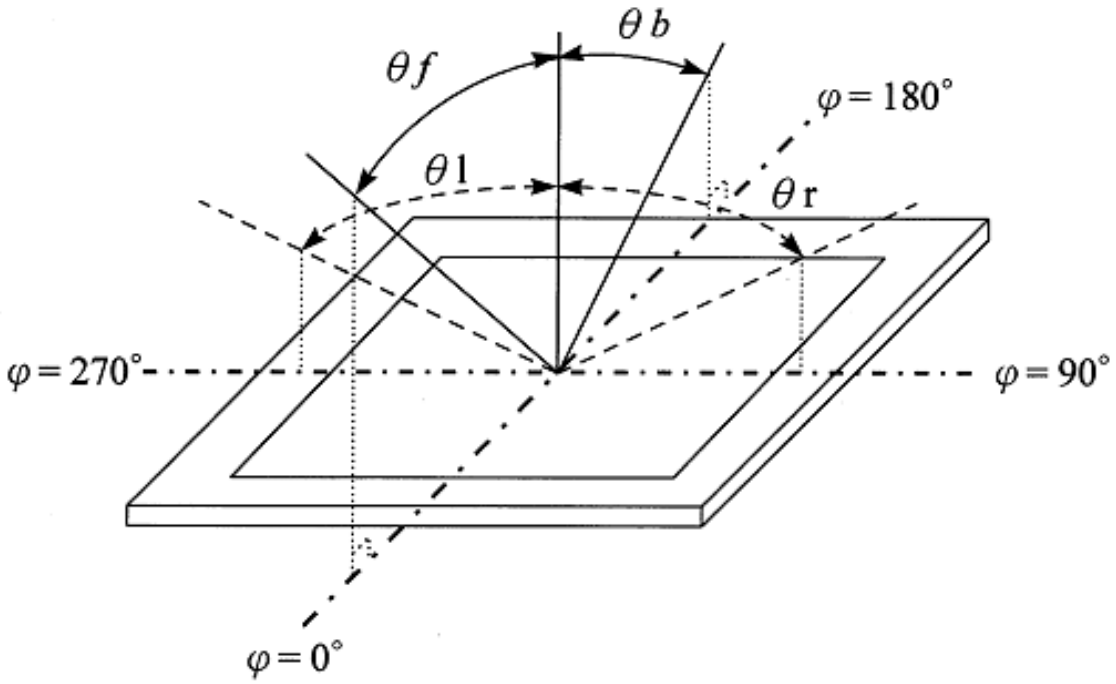
Note1: Definition Operation Voltage (V_{OP}).



Note2: Response time



Note3: Viewing angle



DISPLAY COMMANDS

Table of NT7538 Commands: **(Note)*: ignored data**

Command	A0	/RD	/WR	Code D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio

(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

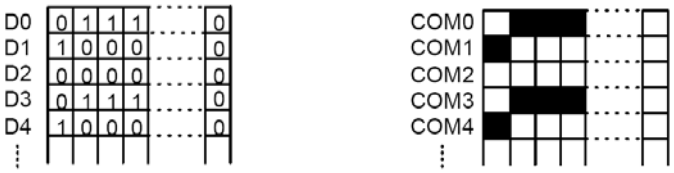
Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

DISPLAY DATA RAM:

The display data RAM is RAM that stores the dot data for the display. It has a 65 (8 page * 8 bit+1)*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7538 chips are used, thus display structures can be created easily with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).

Figure 3



The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address.
Thus, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG131
ADC "0"	0 (H)→	Column Address	→83 (H)
(ADC) "1"	83 (H)←	Column Address	←0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for NT7538, when the common output mode is reversed. The display area is a 65-line area for the NT7538 from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

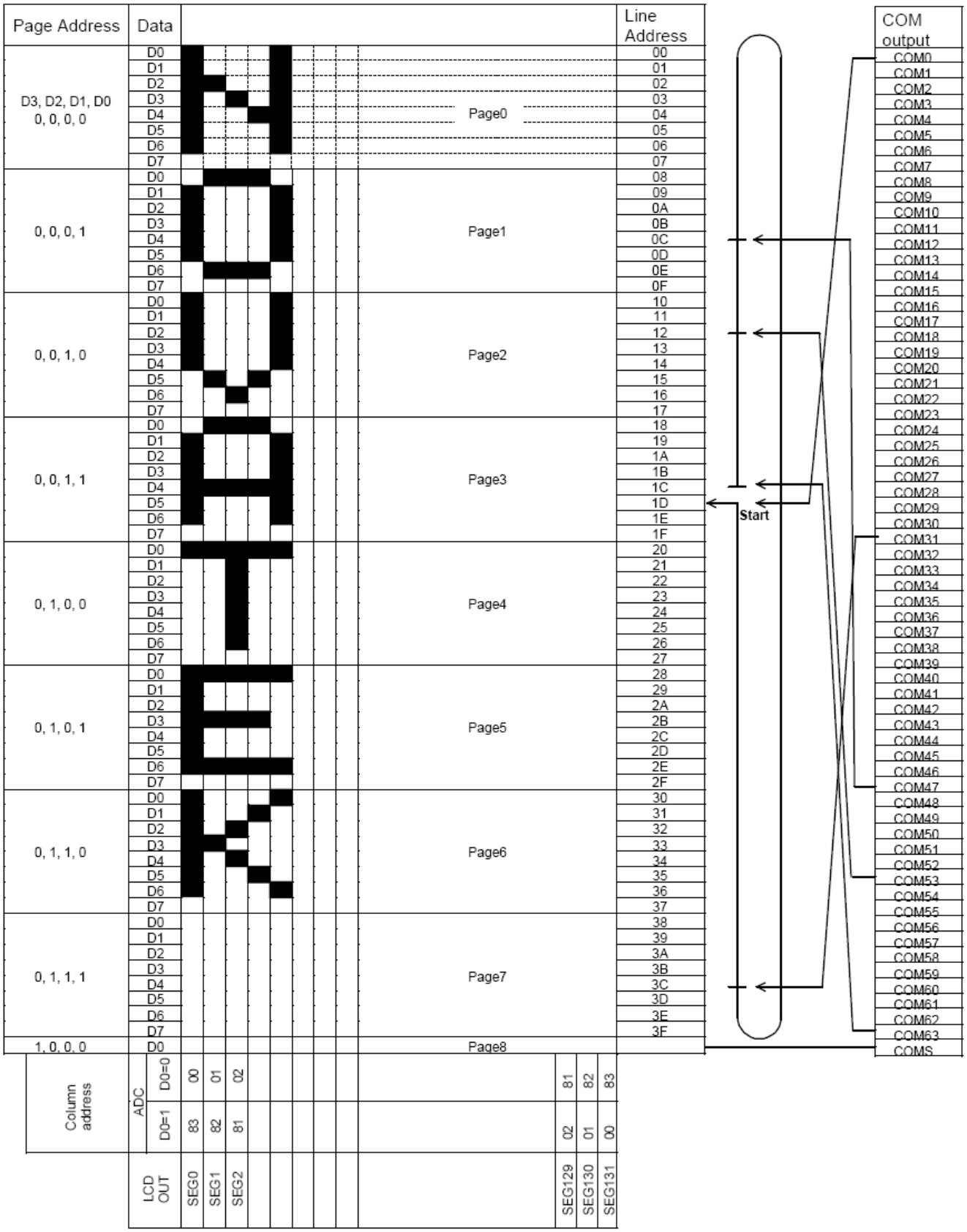
The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H". When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

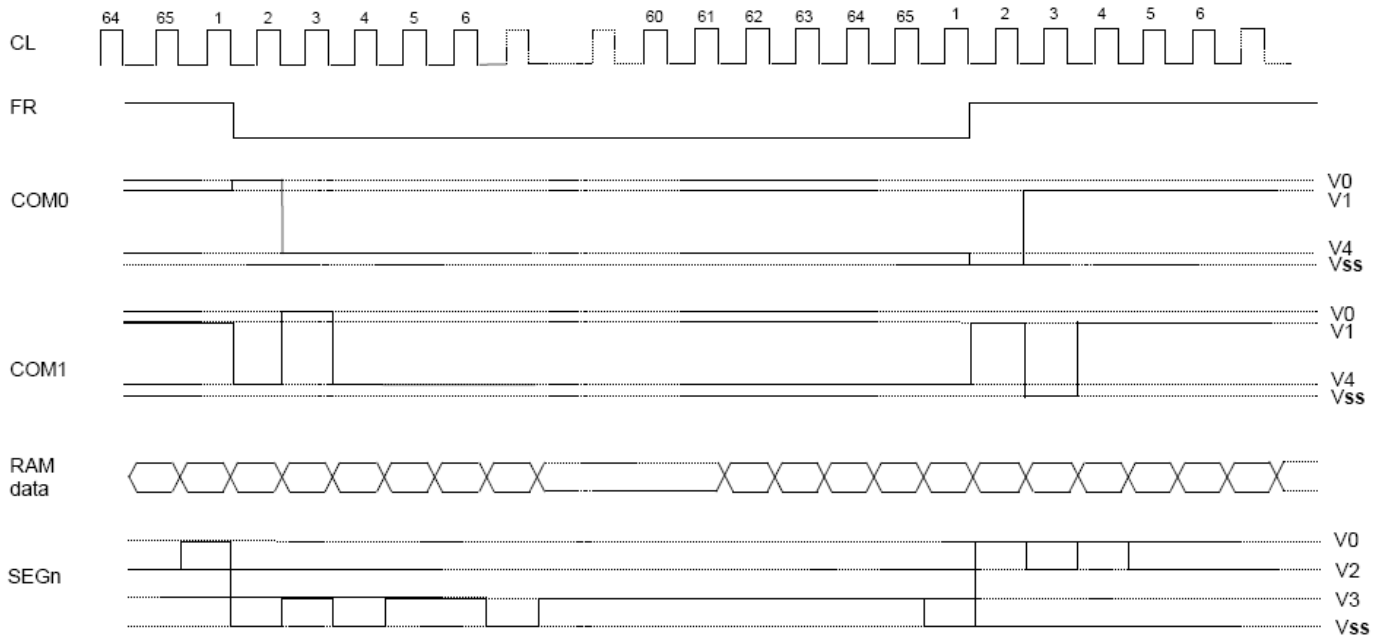
Relationship between display data RAM and address. (if initial display line is 1DH)



Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive waveform using a 2 frames alternating current drive method, as shown in Figure 5, for the liquid crystal drive circuit.

Figure 5



When multiple NT7538 chips are used, the slave chip must be supplied with the display timing signals (FR, CL, /DOF) from the master chip. Table 5 shows the status of the FR, CL, and /DOF signals.

Table 5

Operating Mode		FR	CL	/DOF
Master (M/S = "H")	The internal display oscillator is enabled (CLS = "H")	Output	Output	Output
	The internal display oscillator is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal display oscillator is disabled (CLS = "H")	Input	Input	Input
	The internal display oscillator is disabled (CLS = "L")	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency. fOSC can be selected as 31.4K or 26.3KHz by using Oscilliation Frequency Select command.

Table 6

Duty	Item	fCL	fFR
1/65	On-chip oscillator is used	fOSC/6	fCL/(2 x 65)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 65)
1/49	On-chip oscillator is used	fOSC/8	fCL/(2 x 49)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 49)
1/33	On-chip oscillator is used	fOSC/12	fCL/(2 x 33)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 33)
1/17	On-chip oscillator is used	fOSC/22	fCL/(2 x 17)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 17)
1/9	On-chip oscillator is used	fOSC/44	fCL/(2 x 9)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 9)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table 7

Duty	Status	Common output pads							
		COM [0-15]	COM [16-23]	COM [24-26]	COM [27-36]	COM [37-39]	COM [40-47]	COM [48-63]	COMS
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS
	Reverse	COM[31-16]	NC					COM[15-0]	
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS
	Reverse	COM[47-24]		NC			COM[23-0]		
1/65	Normal	COM[0-63]							COMS
	Reverse	COM[63-0]							

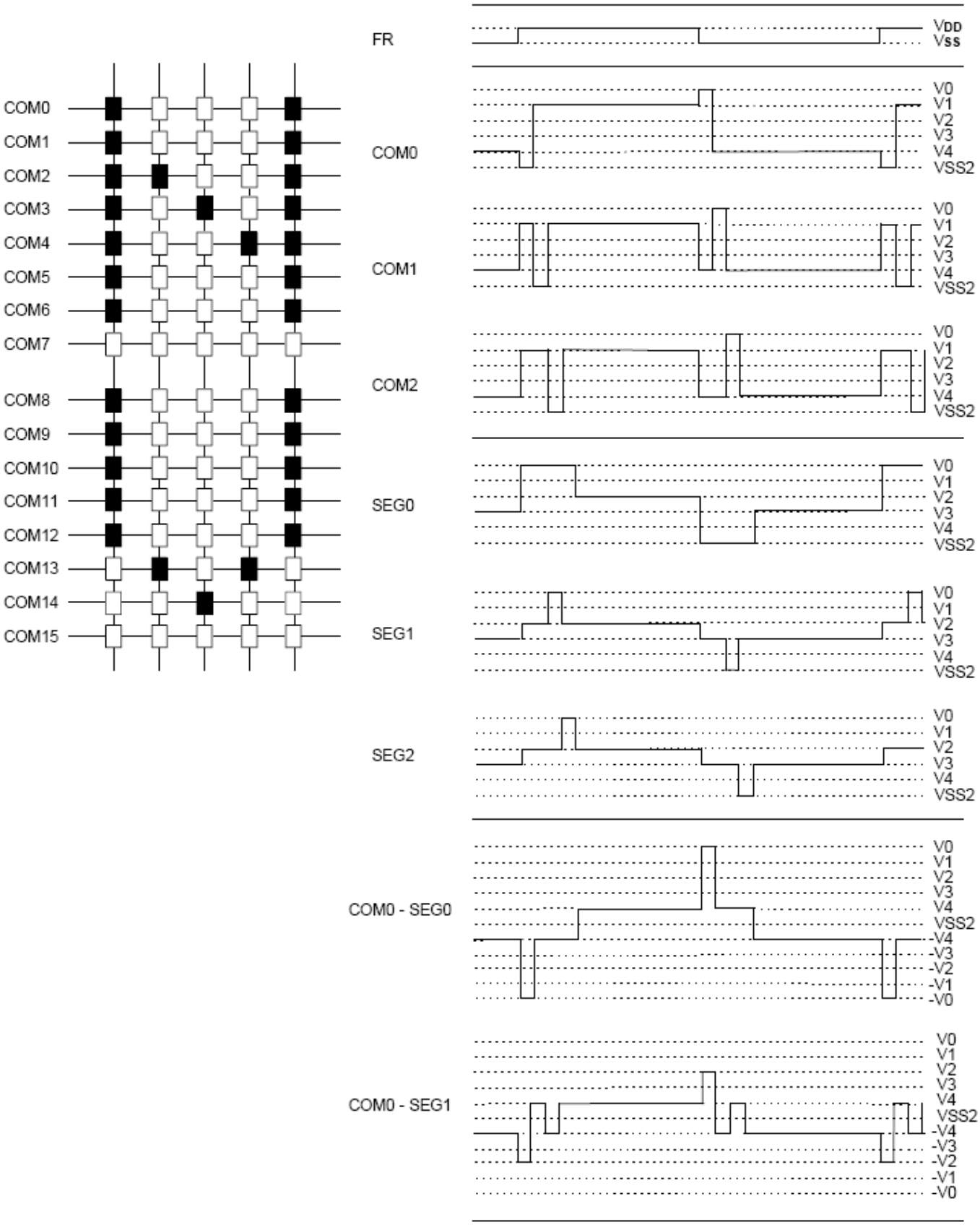
The combination of the display data, the COM scanning signals, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows example of the SEG and COM output waveform.

Configuration Setting

The NT7538 has two optional configurations, configured by DUTY0, DUTY1.

DUTY1, DUTY0	Common	Segment	V1	V2	V3	V4
1, 0 or 1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

Figure 6


COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
Vss
COM0
COM1
COM2
SEG0
SEG1
SEG2
COM0 - SEG0
COM0 - SEG1
V0
V1
V2
V3
V4
VSS2
-V4
-V3
-V2
-V1
-V0

RESET CIRCUIT

When the /RES input falls to “L”, these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF
   Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
    V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. Oscillation frequency 31.4 KHz
17. Normal display mode and frame inversion status (partial display and N-Line inversion release)
18. N-Line inversion register: (D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0), 13-Line inversion
19. Partial start line register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0), the first line
20. DC/DC clock division register: (D3, D2, D1, D0) = (0, 0, 1, 1), fOSC/6
21. Output condition of COM, SEG
    COM: VSS
    SEG: VSS

On the other hand, when the reset command is used, only default settings 7 to 15 above are put into effect. The MPU interface (Reference Example)”, the /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7538, if the internal liquid crystal power supply circuit is not used, user has to supply the external liquid crystal power after the procedure of RESET has been finished (please refer to the timing chart of Reset). During the period of external liquid crystal power supply being supplied, the /RES must be kept “H”. Even though the oscillator circuit operates while the /RES terminal is “L,” the display timing generator circuit is stopped, the FR and FRS terminals are fixed to “H”, the /DOF and CL pins are fixed to “L” only when the intermal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

RELIABILITY TEST CONDITION

No.	TEST Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	70° C 96hrs	------
2	Low temperature storage	Endurance test applying the low storage Temperature for a long time	-20° C 96hrs	-----
3	High temperature operation	Endurance test applying the electric stress (Voltage & current)and the thermal stress to the element for a long time	60° C 96hrs	------
4	Low temperature operation	Endurance test applying the electric stress Under low temperature for a long time	-10° C 96hrs	------
5	High temperature/ Humidity storage	Endurance test applying the electric stress(Voltage & current) and Temperature/ Humidity stress to the element for a long time	40° C 90%RH 96hrs	
6	High temperature/ Humidity operation	Endurance test applying the electric stress (voltage & current)and temperature/ humidity stress to the element for a long time	40° C 90%RH 96hrs	
7	Temperature cycle	Endurance test applying the low and high temperature cycle. -10° C →25° C→60° C 30min←5min←30min.(1 cycle)	-10° C/60° C 10 cycle	------

Supply voltage for logic system = 3.3V. Supply voltage for LCD system = Operating voltage at 25° C.

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	

Environmental condition

The inspection should be performed at the 1metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

PRECAUTION FOR USING LCM MODULE

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
  Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0℃).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

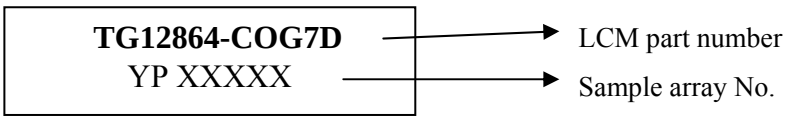
OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections

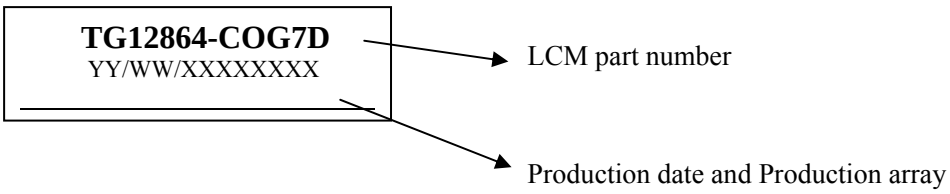
A. DATE CODE RULES

A.1. DATE CODE FOR SAMPLE

YP: meaning sample



A.2. DATE CODE FOR PRODUCTION



A. **TG12864-COG7D** represents LCM part number

C. YY/WW represents Year, Week

YY—Year WW—Week

XXXXXXXX—Production array No.

B. CHANGE NOTES:

Ver.	Descriptions	Editor	Date
V00	First Issue	ZXQ	2013-11-26