EN25LN512

512 Megabit SLC, 3.3 V SPI-NAND Flash Memory

1. Product List

Parameters	Values
V_{CC}	3.3 V
Width	x1, x2 [1], x4
Frequency	104MHz
Internal ECC Correction	1-bit
Transfer Rate	10ns
Loading Throughput	104MT/s
Power-up Ready Time	1ms (maximum value)
Max Reset Busy Time	1ms (maximum value)

2. Features

- Voltage Supply: 3.3V (2.7V ~ 3.6V)
- Organization
  - Memory Cell Array : (64M + 2M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64) Byte
  - Block Erase : (128K + 4K) Byte
- Page Read Operation
  - Page Size : (2K + 64) Byte
  - Read from Cell to Register with Internal ECC: 100us
- Memory Cell: 1bit/Memory Cell
- Support SPI-Mode 0 and SPI-Mode 3 [2]
- Fast Write Cycle Time
  - Page Program Time : 400µs
  - Block Erase Time : 4ms
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Internal ECC Requirement: 1 bit/512 Byte
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years
- Command Register Operation
- NOP: 4 cycles
- OTP Operation
- Bad-Block-Protect
- Package Options
  - 8 contact VDFN (6x8mm)
  - 16 pins SOP 300mil body width
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- Industrial temperature Range

NOTE:
1. x2 PROGRAM operation is not defined.
2. Mode 0: CPOL = 0, CPHA = 1 ; Mode 3: CPOL = 1, CPHA = 1

3. General Description

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. The Eon EN25LN512 is a 512Mb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

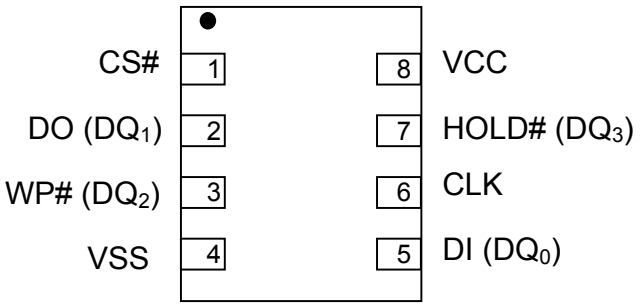
The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to the memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 512 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Each page consists 2112-Byte and is further divided into a 2048-Byte data storage area with a separate 64-Byte spare area. The 64-Byte area is typically used for memory and error management.

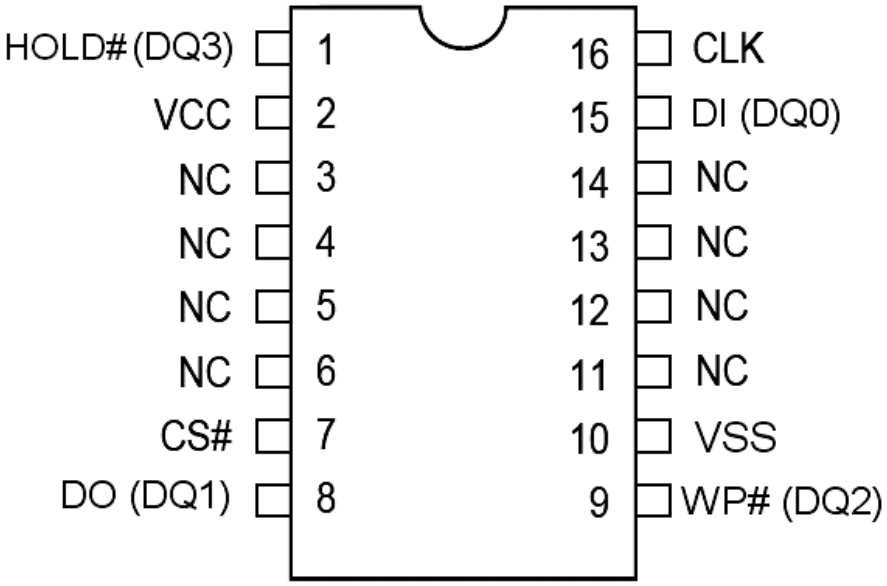
The pins serve as the ports for signals. EN25LN512 has six signal lines plus V_{CC} and ground (GND, V_{SS}). The signal lines are CLK (serial clock), DI (command and data input), DO (response and data output), and control signals CS#, HOLD#, WP#.

4. Package

Figure 1. Pin Configuration

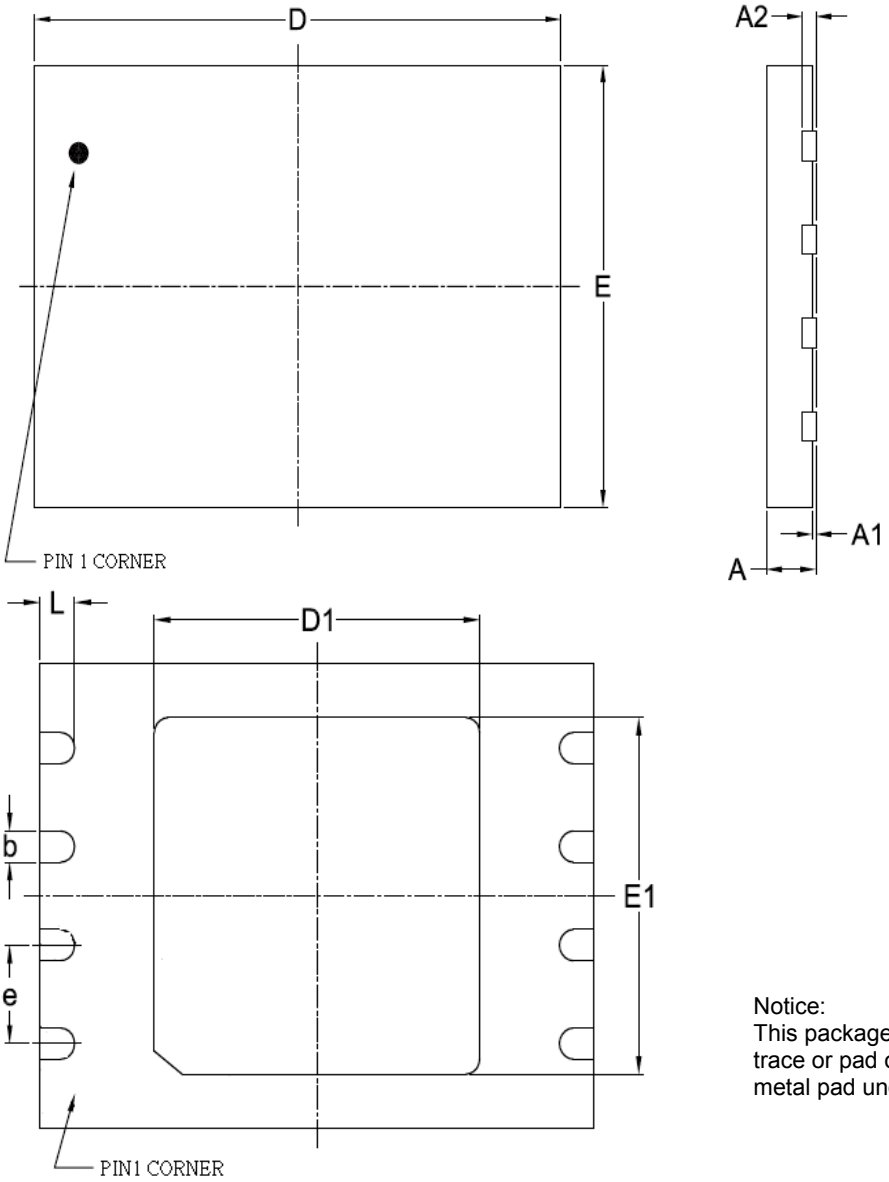


8 - LEAD VDFN



16 - LEAD SOP

Figure 2. VDFN 8 (6x8 mm)

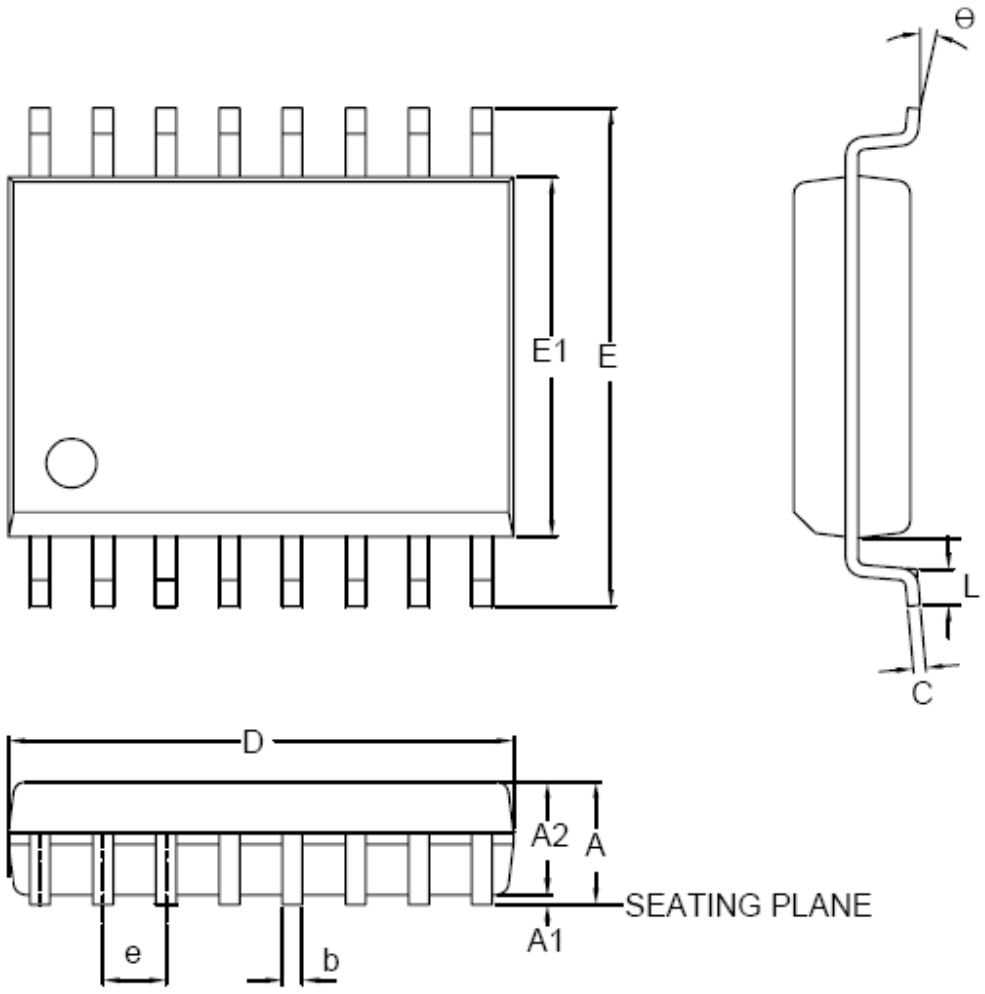


Notice:
This package can't contact to metal trace or pad on board due to expose metal pad underneath the package.

SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	- - -	0.20	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	4.65	4.70	4.75
E1	4.55	4.60	4.65
e	- - -	1.27	- - -
b	0.35	0.40	0.48
L	0.4	0.50	0.60

Note : 1. Coplanarity: 0.1 mm

Figure 3. 16 LEAD SOP 300 mil



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	2.65
A1	0.10	0.20	0.30
A2	2.25	- - -	2.40
C	0.20	0.25	0.30
D	10.10	10.30	10.50
E	10.00	- - -	10.65
E1	7.40	7.50	7.60
e	- - -	1.27	- - -
b	0.31	- - -	0.51
L	0.4	- - -	1.27
θ	0^0	5^0	8^0

Note : 1. Coplanarity: 0.1 mm

5. Pin Description

Symbol	Pin Name	Function
CS#	Chip Select (Input)	The device is activated[1] /deactivated[2] as CS# is driven LOW/HIGH. After power-on, the device requires a falling-edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
HOLD# (DQ_3)	Hold (Input) /DQ_3 (Input/Output)	Hold pauses[3] any serial communication with the device without deselecting it. When driven LOW, DO is at high impedance (Hi-Z), and all inputs in DI and CLK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation.
WP# (DQ_2)	Write Protect (Input) / DQ_2 (Input/Output)	WP# is driven LOW to prevent overwriting the block-lock bits (BP0, BP1, and BP2) if the block register write disable (BRWD) bit is set.[4] WP# must not be driven during x4 operation.
CLK	Serial Clock (Input)	CLK provides serial interface timing. Address, commands, and data in DI are latched on the rising edge of CLK. Output (data in DO) is triggered after the falling-edge of CLK. The clock is valid only when the device is active.[5]
DI (DQ_0)	Serial Data Input (Input) / DQ_0 (Input/Output)	DI transfers data serially into the device. Device latches addresses, commands, and program data in DI on the rising-edge of CLK. DI must not be driven during x2 or x4 READ operation.
DO (DQ_1)	Serial Data Output (Output) / DQ_1 (Input/Output)	DO transfers data serially out of the device on the falling-edge of CLK. DO must not be driven during x2 or x4 PROGRAM operation.
V_{CC}[6]	Power	V_{CC} is the power supply for device.
V_{SS}[6]	Ground	Ground
N.C.	No Connection	Not internally connected.

Note:
1. CS# places the device in active power mode.
2. CS# deselects the device and places DO at high impedance.
3. It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
4. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can't be altered.
5. DI and DO can be triggered only when the clock is valid.
6. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

6. Block Diagram

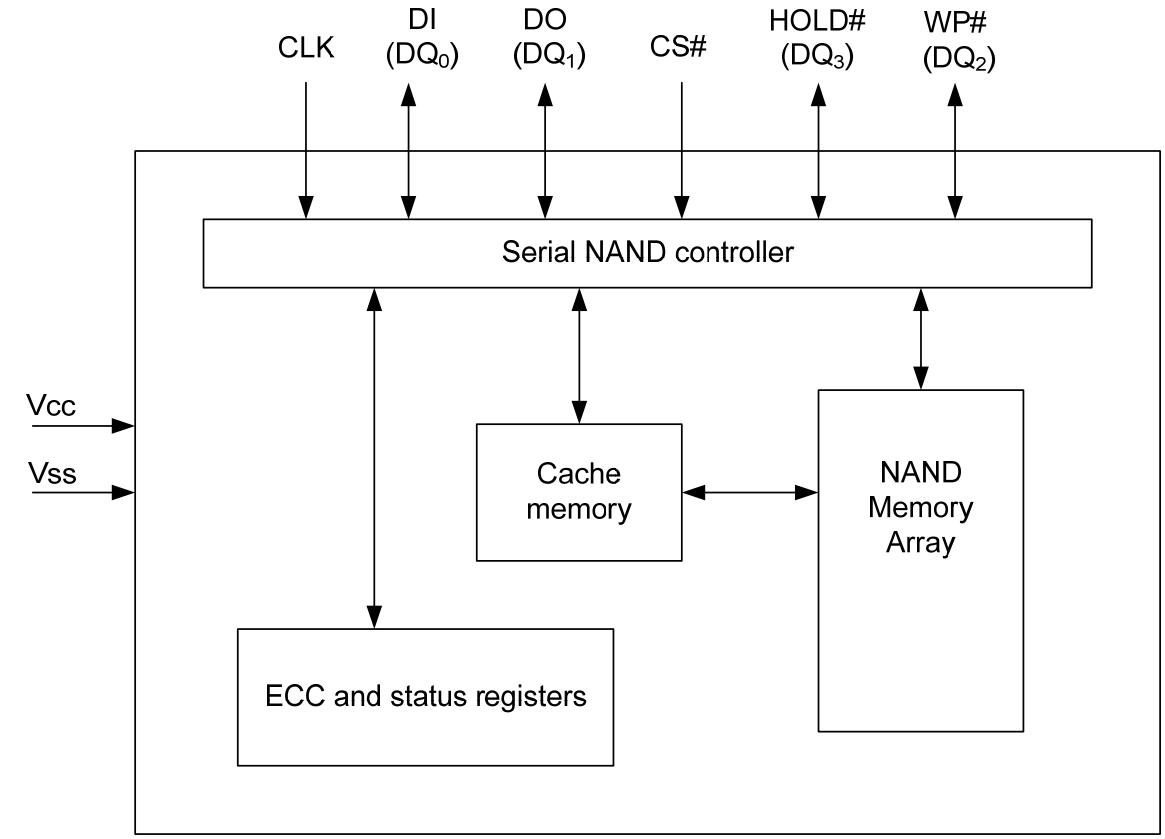


Figure 4. Functional Block Diagram

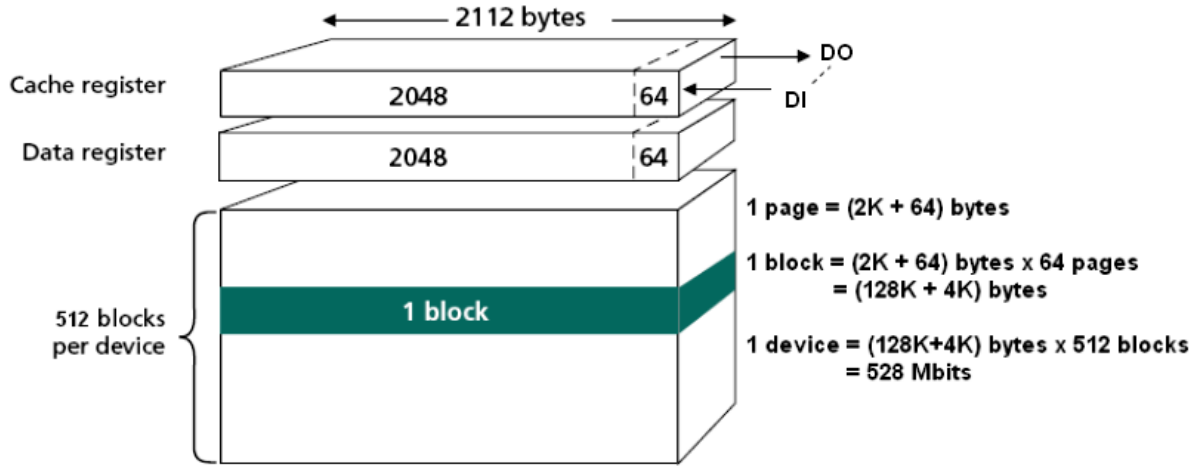


Figure 5. Array Organization

7. Command Set

Table 1. Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes
BLOCK ERASE	D8h	3	0	0
GET FEATURE [1]	0Fh	1	0	1
SET FEATURE	1Fh	1	0	1
WRITE DISABLE	04h	0	0	0
WRITE ENABLE	06h	0	0	0
PROGRAM LOAD	02h	2	0	1 to 2112
PROGRAM LOAD x4 [2]	32h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112
PROGRAM LOAD RANDOM DATA x4 [2]	34h	2	0	1 to 2112
PROGRAM EXECUTE	10h	3	0	0
PAGE READ	13h	3	0	0
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112
READ FROM CACHE x2	3Bh	2	1	1 to 2112
READ FROM CACHE x4 [2]	6Bh	2	1	1 to 2112
READ ID [3]	9Fh	1	0	2
RESET	FFh	0	0	0

Note:
1. Refer to Feature Register.
2. Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.
3. Address is 00h to get JEDEC ID

8. Parameters

8.1. Absolute Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	V_{IN}	-0.6 to +4.6	
	$V_{I/O}$	-0.6 to VCC + 0.3 (< 4.6)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2. Recommended Operating Conditions

(Voltage reference to GND, T_A = – 40°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

8.3. DC and Operation Conditions

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ. [2]	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	fC =104MHz, CS# =V_{IL}, I_{OUT} =0mA, TBD	-	12	20	mA
	Program	I_{CC2}	-	-	12		
	Erase	I_{CC3}	-	-	12		
Stand-by Current (TTL)		I_{SB1}	CS# =V_{IH}, WP# =0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CS# = V_{CC} -0.2, WP# =0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN} =0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH} [1]	-	0.7 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL} [1]	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = -20uA	0.7 x V_{CC}	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} =1mA	-	-	0.15 V_{CC}	V

Note:
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to VCC + 0.4V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

8.4. Valid Block and Error Management

Description	Requirement
Minimum / Maximum number of valid block number of block	502 / 512
Bad block mark	non FFh
Mark location	Column 2048 of page 0 and page 1

Note:
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.

2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

8.5. AC Test Condition

(T_A = – 40°C to 85°C, V_{CC}=2.7V~3.6V, unless otherwise noted)

Parameter	Condition
Input Pulse Levels	0.2 V_{CC} to 0.8 V_{CC}
Input Rise and Fall Times	Max: 2.4 ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L= 15pF

8.6. Capacitance

(T_A = 25°C, V_{CC}=3.3V, f =1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

8.7. Read / Program / Erase Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average Program Time	t_{PROG}	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	4	10	ms
Data Transfer from Cell to Register with Internal ECC	t_{RD}	-	-	100	us

8.8. General Timing Characteristic

Parameter	Symbol	Min	Max
Clock frequency	f_C		104MHz
Hold# non-active hold time relative to CLK	t_{CD}	5ns	
Hold# hold time relative to CLK	t_{CH}	5ns	
Command deselect time	t_{CS}	100ns	
CS# setup time	t_{CSS}	5ns	
CS# hold time	t_{CSH}	5ns	
The last valid Clock low to CS# high	t_{CSCL}	5ns	
Output disable time	t_{DIS}		20ns
Hold# non-active setup time relative to CLK	t_{HC}	7ns	
Hold# setup time relative to CLK	t_{HD}	5ns	
Data input setup time	t_{SUDAT}	2ns	
Data input hold time	t_{HDDAT}	5ns	
Output hold time	t_{HO}	0ns	
Hold# to output Hi-Z	t_{HZ}		15ns
Hold# to output Low-Z	t_{LZ}		15ns
Clock low to output valid	t_V		8ns
Clock high time	t_{WH}	4.5ns	
Clock low time	t_{WL}	4.5ns	
Clock rise time (slew rate)	t_{CRT}	0.1V/ns	
Clock fall time (slew rate)	t_{CFT}	0.1V/ns	
WP# setup time	t_{WPS}	20ns	
WP# hold time	t_{WPH}	100ns	
Resetting time during Idle/Read/Program/Erase	t_{RST}		5/100/900/500us

Note: For first RESET condition after power up, tRST will be 1ms MAX.

9. Technical Notes

9.1. Bus Operation

SPI NAND supports two SPI modes:

(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0

(Mode 3) CPOL=1, CPHA=1

Input data is latched in on the rising edge of CLK, and output data is available from the falling edge of CLK for both modes.

When CS# is high, keep CLK at V_{CC} (Mode 0) or V_{SS} (Mode 3). Do not begin toggling CLK until after CS# is driven LOW.

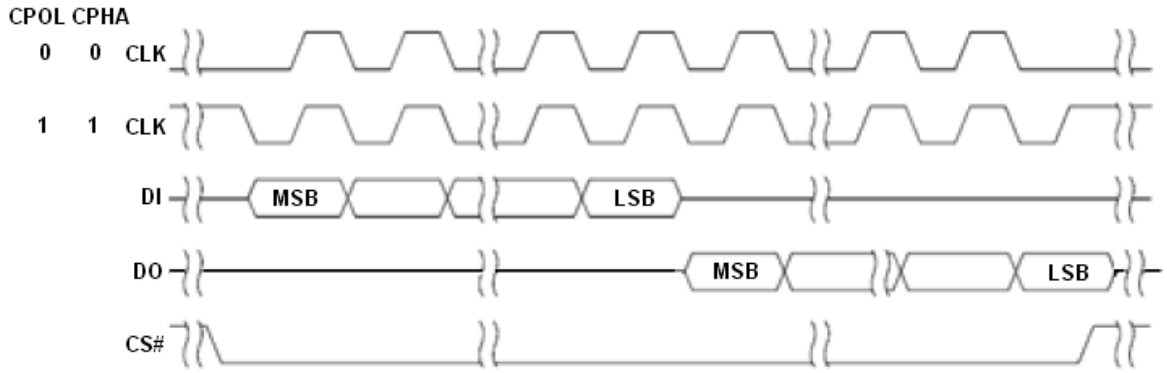


Figure 6. SPI Modes Timing

9.2. Feature Operations

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.
When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in Table 2, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 2. Feature Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0h	BRWD [1]	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	ECC Enable [2]	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL [3]	OIP
Output Driver	D0h [4]	Reserved	DRV_S1	DRV_S0	Reserved	Reserved	Reserved	Reserved	Reserved

Note:
1. BRWD is not protected (fixed) even when BRWD is enabled and WP# is LOW; (38h) is the default data byte value for Block Lock Register after power-up.
2. 1-bit internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1) or disabled (ECC enable = 0); (10h) is the default data byte value for OTP Register after power-up.
3. WEL = 0 is the default data bit value for Status Register after power-up.
4. (20h) is the default data byte value for Output Driver Register after power-up.

Table 3. Block Protect Bits of Block Lock Register

BP2 (5)	BP1 (4)	BP0 (3)	Protected Rows
0	0	0	None; all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

9.3 One-Time Programmable (OTP) Operations

This Eon flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area. It means the OTP area becomes read-only after being locked.

The OTP area is only accessible while the OTP enable bit is set to 1. To set the device to OTP operation mode, issue the Set Feature (1Fh) command. When the device is in OTP operation mode, subsequent Read and/or Page Program (both X1 and X4) are applied to the OTP area. Please refer to relative command sequences defined in datasheet. When you want to come back to normal operation, you need to set OTP enable bit to 0. Otherwise, device will stay in OTP mode.

OTP Read:

- **Issue the Set Feature (1Fh) command.**
- **Issue the feature address (B0h).**
- **Set the OTP enable bit to 1.**
- **Issue the Page Read (13h) command.**

OTP Program:

- **Issue the Set Feature (1Fh) command.**
- **Issue the feature address (B0h).**
- **Set the OTP enable bit to 1.**
- **Issue the Write Enable (06h) command.**
- **Issue the Program Load (02h) and Program Execute (10h) commands.**

OTP Lock

- **Issue the Set Feature (1Fh) command.**
- **Issue the feature address (B0h).**
- **Set both the OTP enable and OTP protect bits to 1.**
- **Issue the Program Execute (10h) command.**

Table 4. OTP Modes and Commands

		Set Feature
OTP Operation mode	Read	1Fh - B0h[1] - 40h or 50h[2]
	Page Program	1Fh - B0h - 40h or 50h
OTP Protection mode	Program Protect	1Fh - B0h - C0h or D0h
OTP Release mode	Leave OTP mode	1Fh - B0h - 00h or 10h

Note:
1. B0h is OTP status register address.
2. 40h (**50h**), 00h (**D0h**), and 00h (**10h**) are OTP register data values as ECC disabled (**enabled**).

Table 5. OTP Area Details

Description	Value
Number of OTP pages	30
OTP pages address	00h – 1Dh
Number of partial page programs for each page in the OTP area	1

Table 6. OTP State Bits of OTP Register

OTP Protect Bit (7)	OTP Enable Bit (6)	State
0	0	Normal operation (read array)
0	1	Access OTP space
1	0	Not applicable
1	1	Lock the OTP area

Table 7. Driver Strength Bits of Output Driver Register

DRV_S1	DRV_S0	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

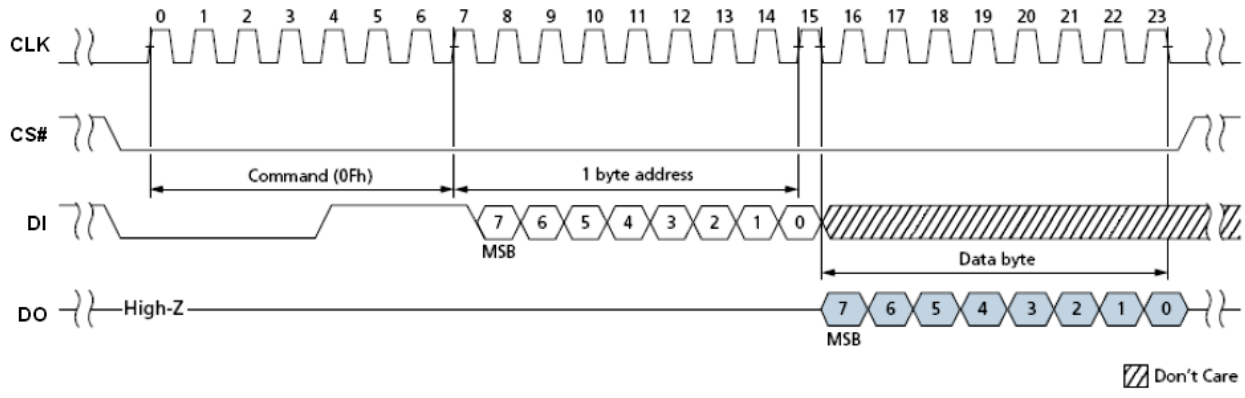


Figure 7. GET FEATURE (0Fh) Timing

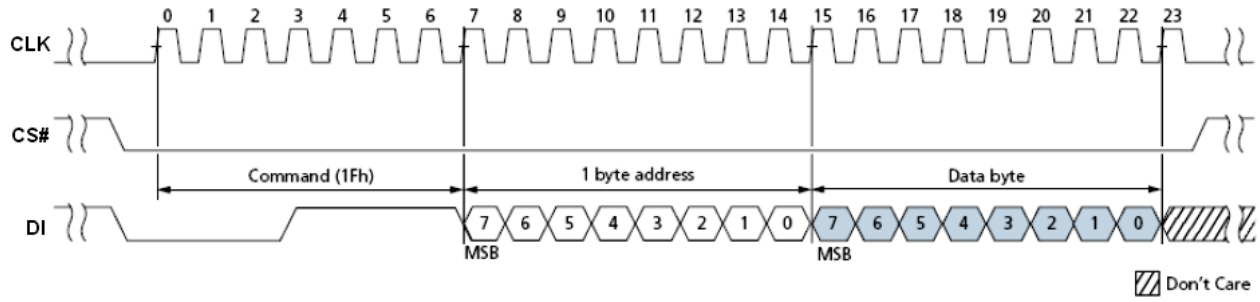


Figure 8. SET FEATURE (1Fh) Timing

9.3. Array Write Enable / Disable

The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This is required in the following WRITE operations that change the contents of the memory array: PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

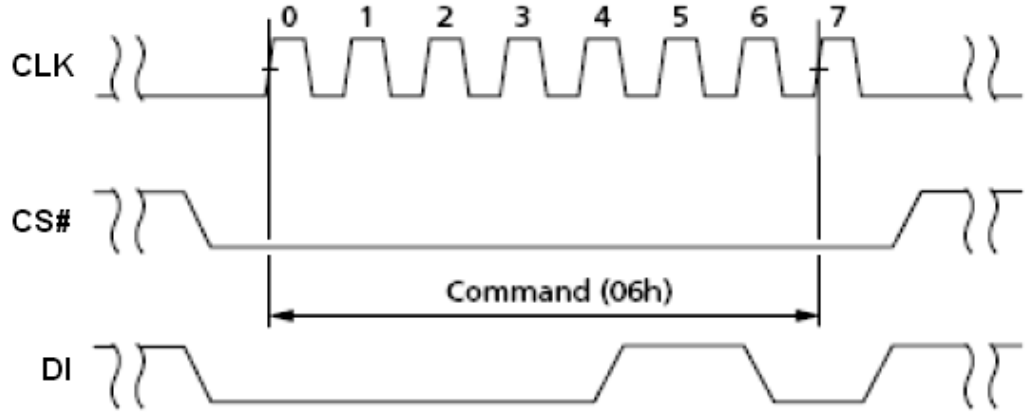


Figure 9. WRITE ENABLE (06h) Timing

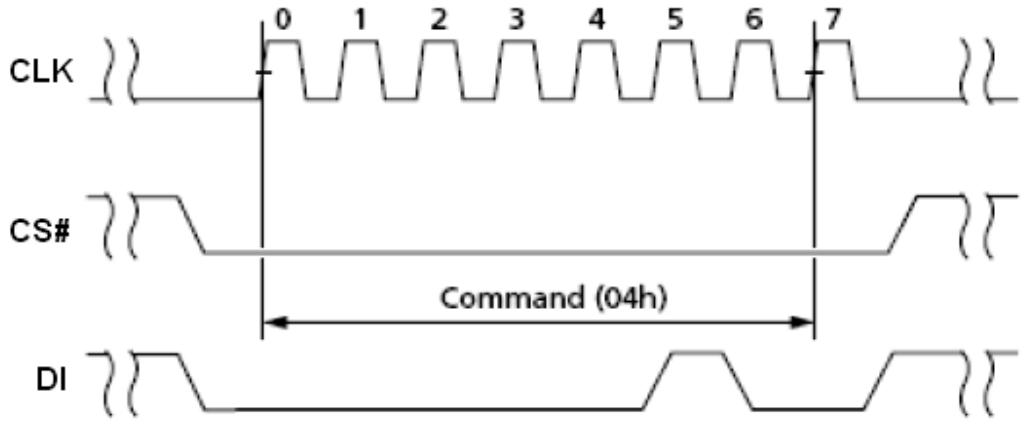


Figure 10. WRITE DISABLE (04h) Timing

9.4. Status Register

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation, refer to Table 2, Table 6 and Table 7.

Table 8. Bits of Status Register

Bit Name	Mode	Description
Program fail (Bit 3)	R	P_Fail is set to 1 as a program failure has occurred. P_Fail = 1 will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to 0 during the PROGRAM EXECUTE command sequence or the RESET command.
Erase fail (Bit 2)	R	E_Fail is set to 1 as an erase failure has occurred. E_Fail = 1 will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to 0 at the start of the BLOCK ERASE command sequence or the RESET command.
Write enable latch (Bit1)	W	WEL must be set to 1 to indicate the current status of the write enable latch, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE command. WEL is disabled (WEL=0) by issuing the WRITE DISABLE command.
Operation in progress (Bit 0)	R	OIP is set to 1 when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing. OIP is cleared to 0 as the interface is in ready state.
ECC_Status1 (Bit 5) ECC_Status0 (Bit 4)	R	Table 8 shows the ECCS definitions. ECC_S is set to 00h either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC_S is invalid if ECC is disabled (via a SET FEATURE command to Bit 4 in OTP register).

Table 9. ECC Status Bits of Status Register

ECCS1 (5)	ECCS0 (4)	Description
0	0	No errors
0	1	1-bit error detected and corrected
1	0	2-bit errors detected and not corrected
1	1	Reserved

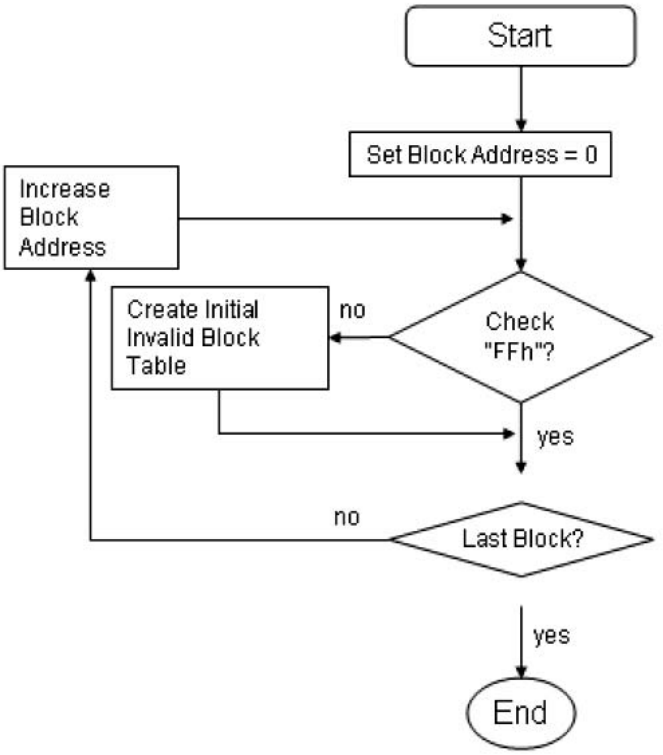
9.5. Error Management

Mask Out Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Eon. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid blocks have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block does not affect the performance of valid blocks because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid blocks via address mapping.
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial invalid Blocks

Unpredictable behavior may result from programming or erasing the defective blocks. Figure 11 illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.
A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address 2048 of page 0 and page 1. If the read data is not FFh, the block is interpreted as an invalid block. Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.



Check "FFh" at column address 2048 of the first page and the second page

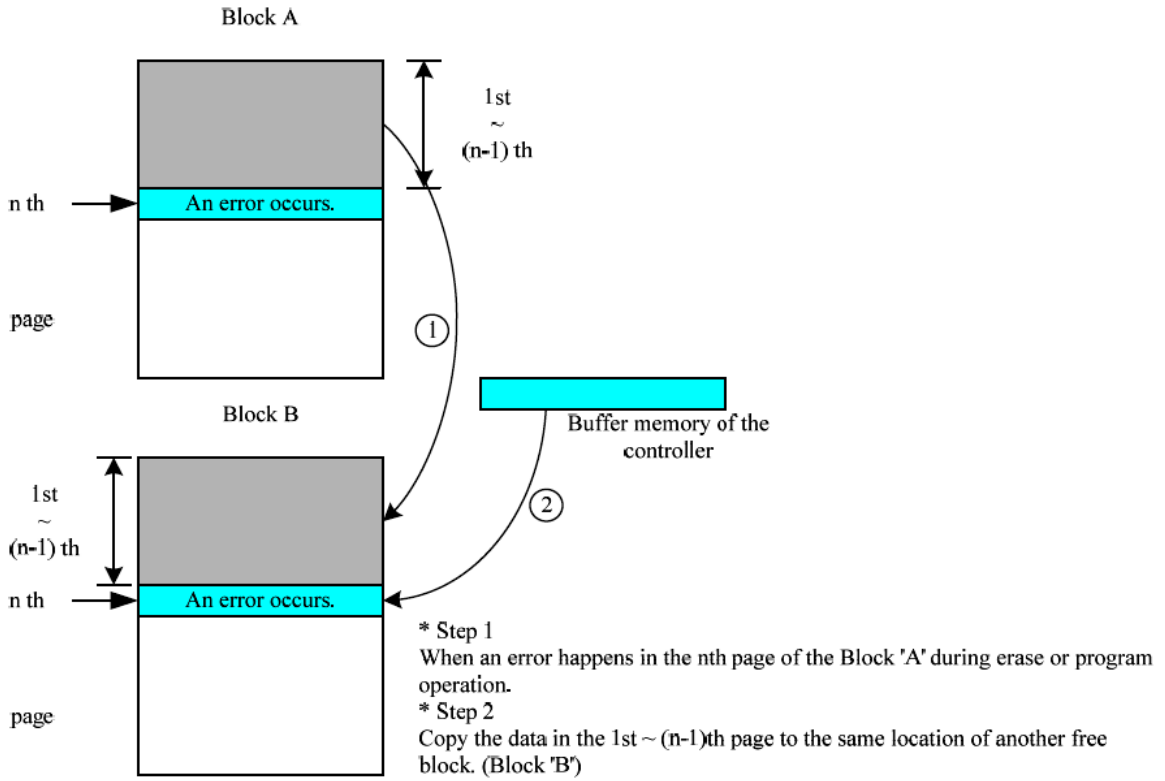
```
For (i=0; i<Num_of_LUs; i++)
{
    For (j=0; j<Blocks_Per_LU; j++)
    {
        Defect_Block_Found=False;

        Read_Page(lu=i, block=j, page=0);
        If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

        Read_Page(lu=i, block=j, page=1);
        If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

        If (Defect_Block_Found)   Mark_Block_as_Defective(lu=i, block=j);
    }

 }
```

Figure 11. Algorithm for Bad Block Scanning

Block Replacement

Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in status register, block replacement should be done. Because PROGRAM status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.



Note: Please refer to Internal Data Move.

ECC Protection

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state.
During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output bus.

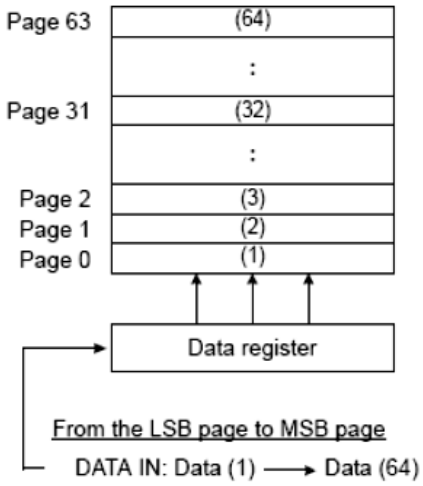
Table 10. ECC Protection

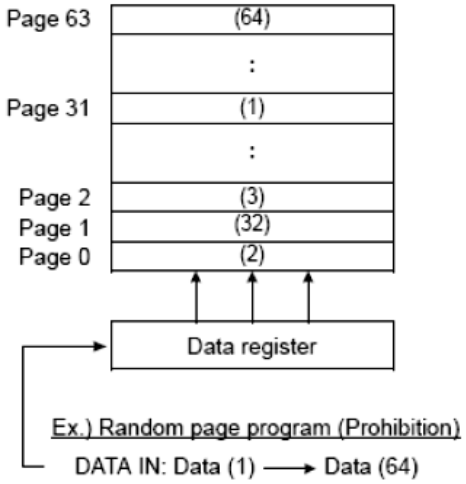
Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh (511)	000h (0)	Yes	Main 0	User data 0 [1]
3FFh (1023)	200h (512)	Yes	Main 1	User data 1 [1]
5FFh (1535)	400h (1024)	Yes	Main 2	User data 2 [1]
7FFh (2047)	600h (1536)	Yes	Main 3	User data 3 [1]
800h (2048)	800h (2048)	No		Reserved
803h (2051)	801h (2049)	No		ECC for main 0 [2]
807h (2055)	804h (2052)	Yes		ECC for spare 0 [2]
80Fh (2063)	808h (2056)	Yes	Spare 0	User meta data 0 [1]
810h (2064)	810h (2064)	No		Reserved
813h (2067)	811h (2065)	No		ECC for main 1 [2]
817h (2071)	814h (2068)	Yes		ECC for spare 1 [2]
81Fh (2079)	818h (2072)	Yes	Spare 1	User meta data 1 [1]
820h (2080)	820h (2080)	No		Reserved
823h (2083)	821h (2081)	No		ECC for main 2 [2]
827h (2087)	824h (2084)	Yes		ECC for spare 2 [2]
82Fh (2095)	828h (2088)	Yes	Spare 2	User meta data 2 [1]
830h (2096)	830h (2096)	No		Reserved
833h (2099)	831h (2097)	No		ECC for main 3 [2]
837h (2103)	834h (2100)	Yes		ECC for spare 3 [2]
83Fh (2111)	838h (2104)	Yes	Spare 3	User meta data 3 [1]
FFFh (4095)	840h (2112)	No		Reserved

Note:
1. The user areas must be programmed within a single partial-page programming operation so the NAND Flash device can calculate the proper ECC bytes.
2. When internal ECC is enabled, these areas are prohibited to be programming.

9.6. Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





10. Operations and Timing Diagrams

10.1. Read Operations and Serial Output

The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1) / 3Bh (x2) / 6Bh (x4)

PAGE READ command requires 24-bit address with 9 dummy and a 15-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

READ FROM CACHE command requires 16-bit address with 4 dummy bits and a 12-bit column address for the starting byte. The starting byte can be 0 to 2011, but after the end of the cache register is reached, the data does not wrap around and DO goes to a Hi-Z state.

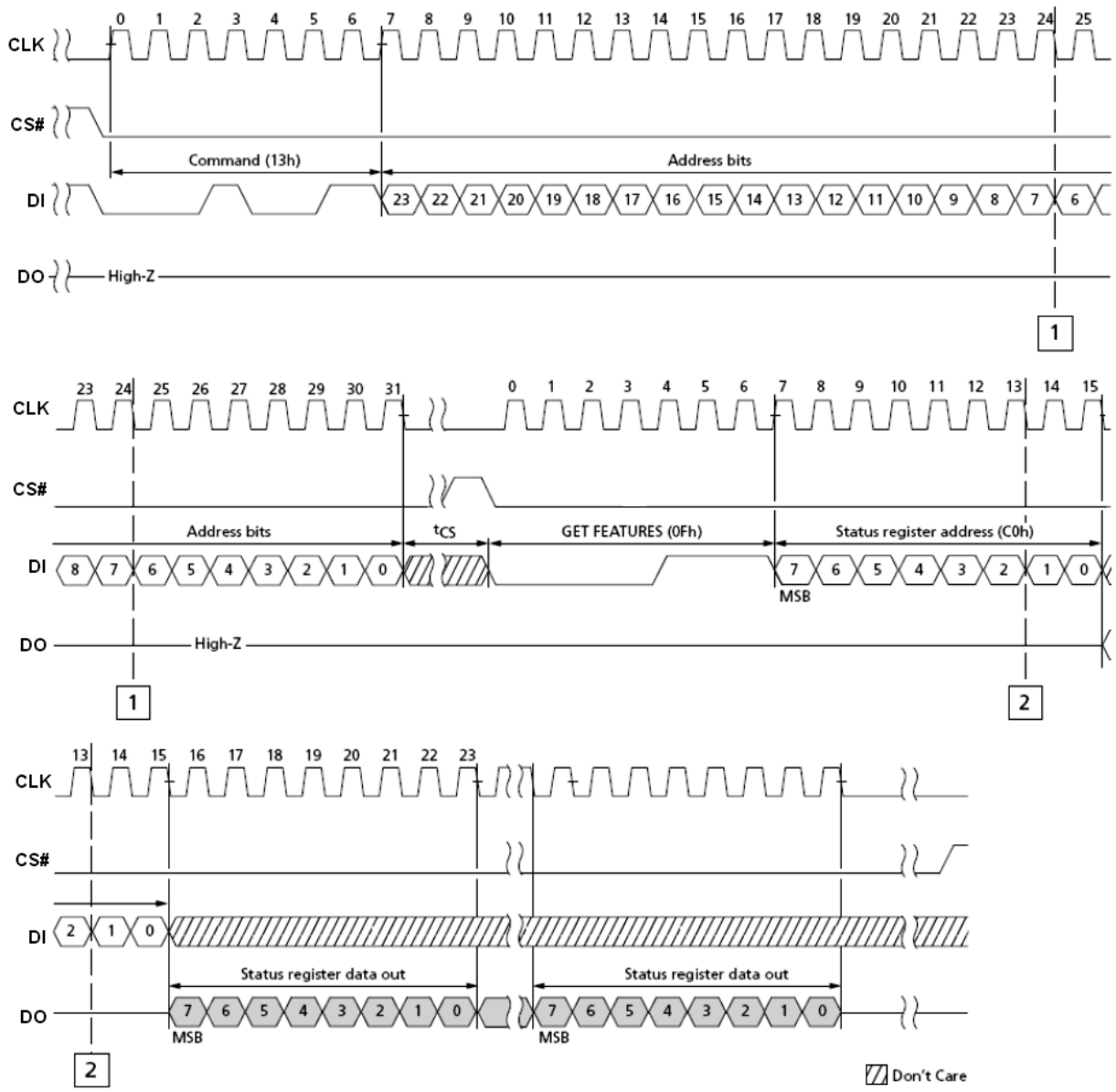


Figure 12. PAGE READ (13h) Timing

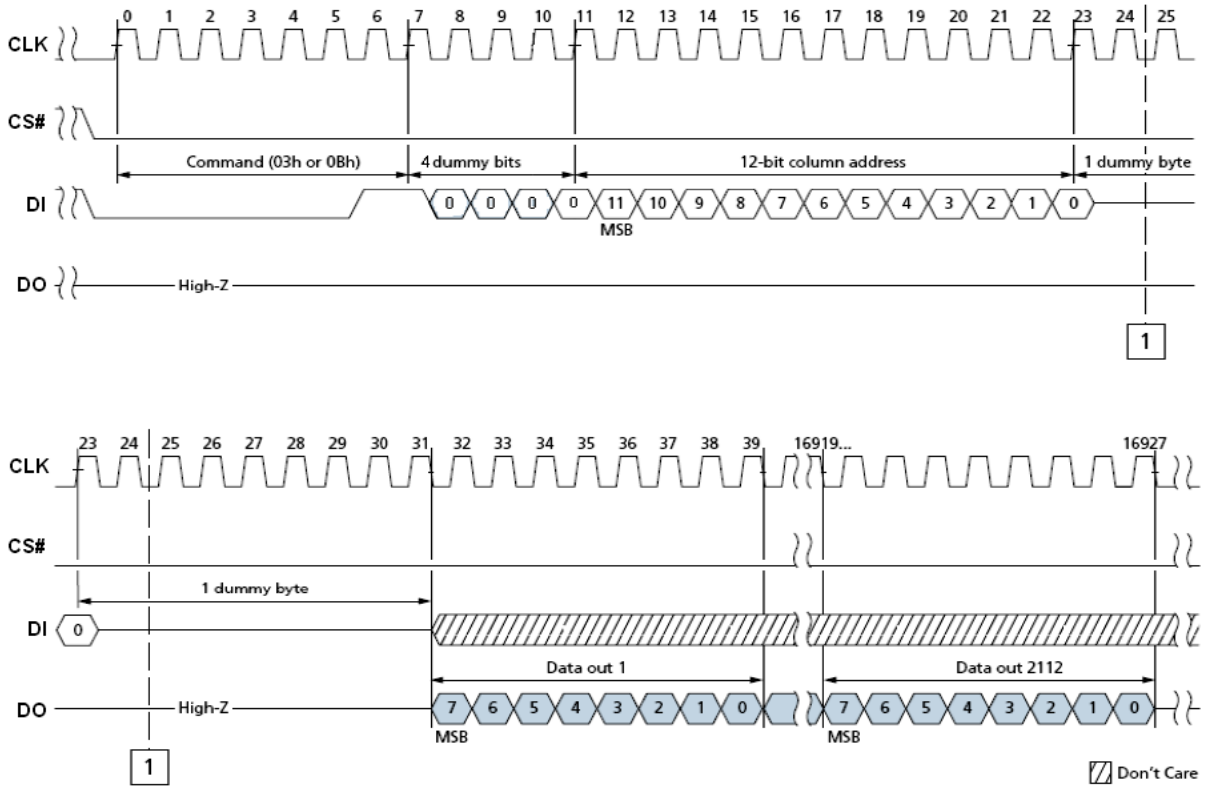


Figure 13. READ FROM CACHE (03h or 0Bh) Timing

Note: Final data (LSB in the 2112th Byte for x1) would be reset to Hi-Z at CLK rising edge.

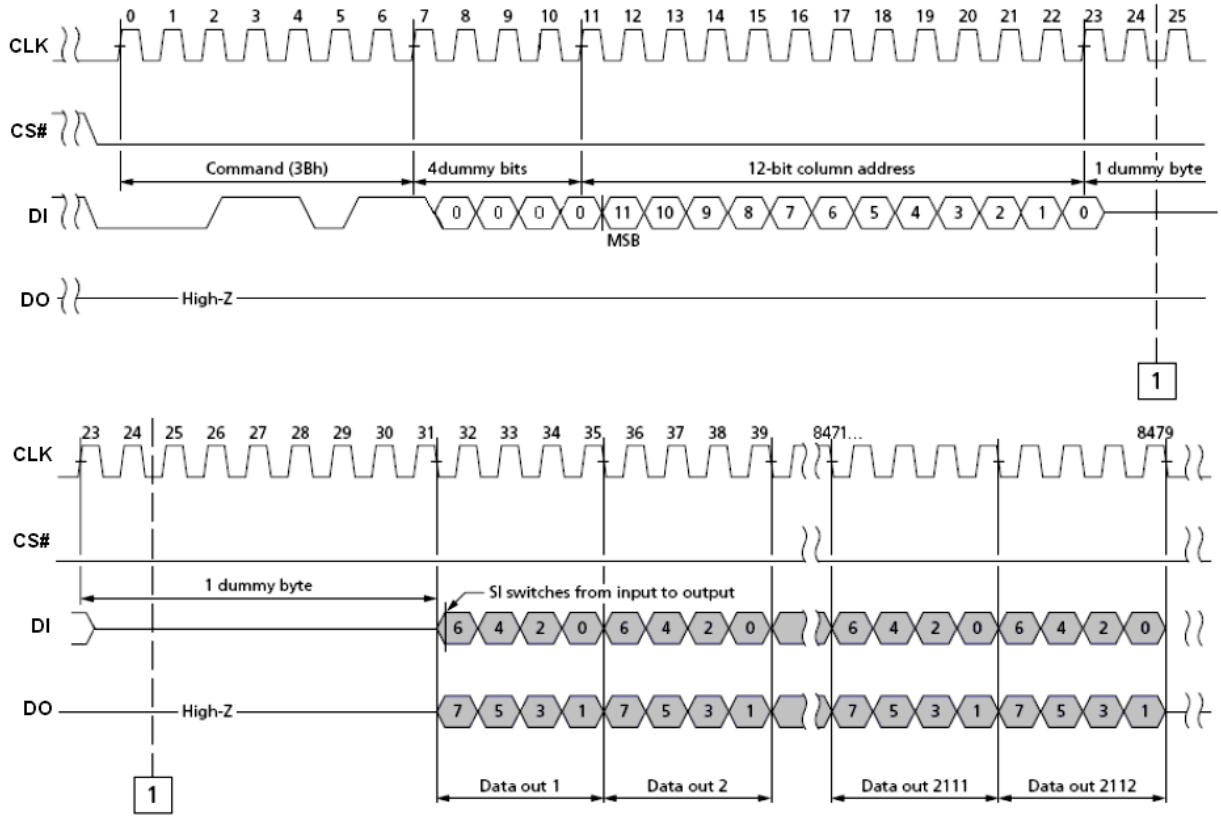


Figure 14. READ FROM CACHE x2 (3Bh) Timing

Note: Final data (last 2-bit in the 2112th Byte for x2) would be reset to Hi-Z at CLK rising edge.

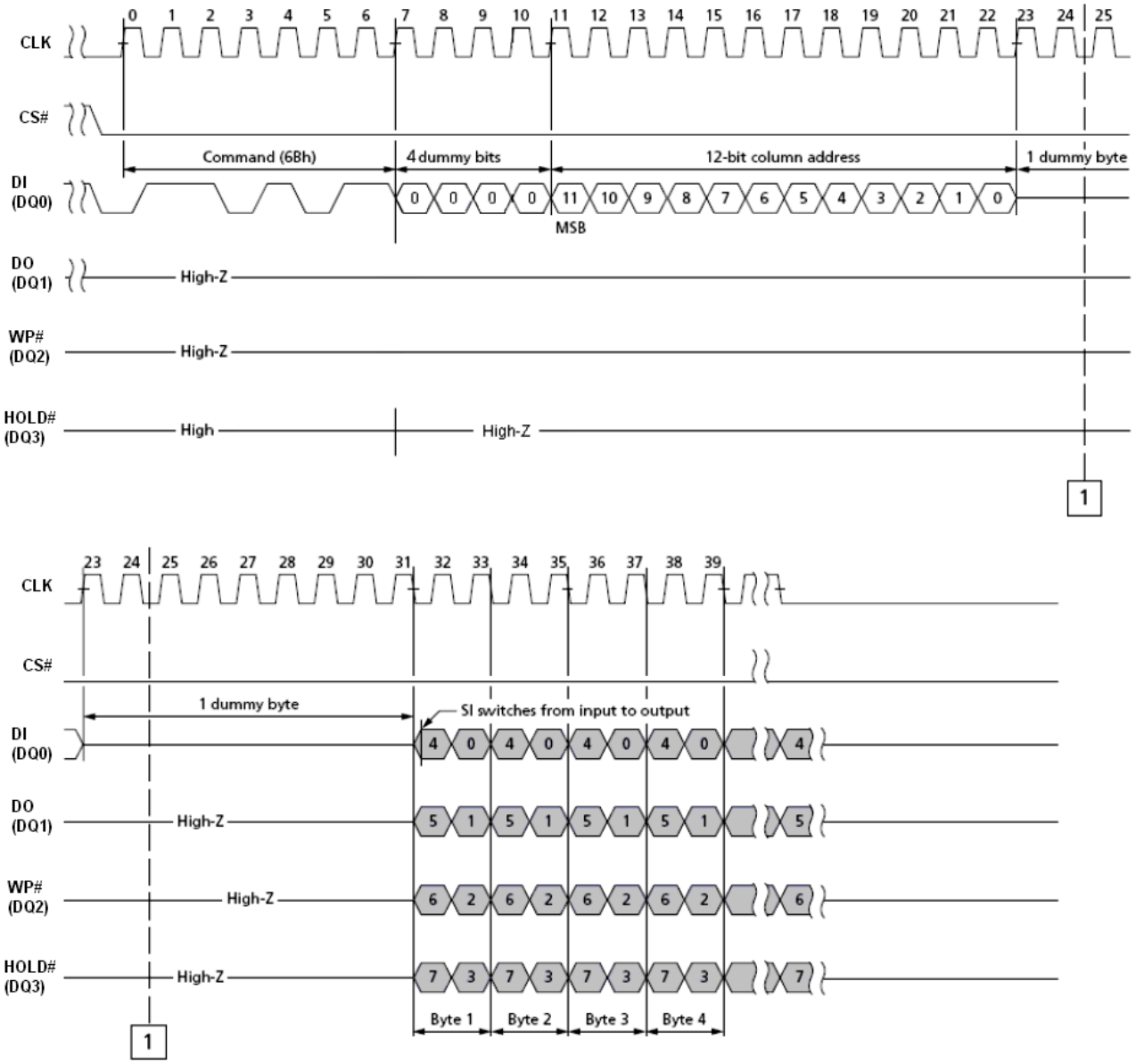


Figure 15. READ FROM CACHE x4 (6Bh) Timing

Note: Final data (last 4-bit in the 2112th Byte for x4) would be reset to Hi-Z at CLK rising edge.

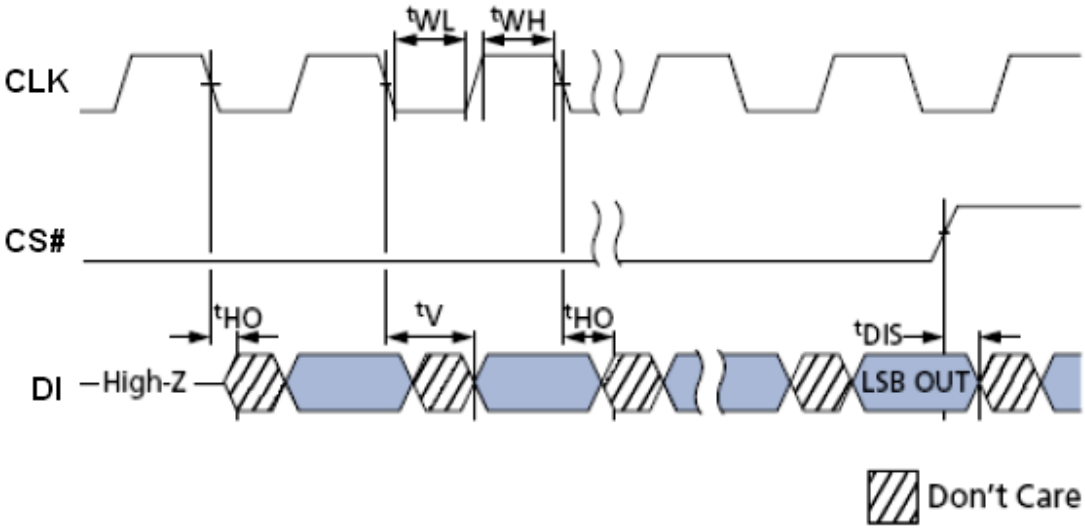


Figure 16. Serial Output Timing

10.2. Program Operations and Serial Input

Page Program

The command sequence is follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The page program operation sequence programs 1 byte to 2112 bytes of data within a page. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register. After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for tPROG time. PROGRAM EXECUTE command requires 24-bit address with 9 dummy bits and a 15-bit row address.

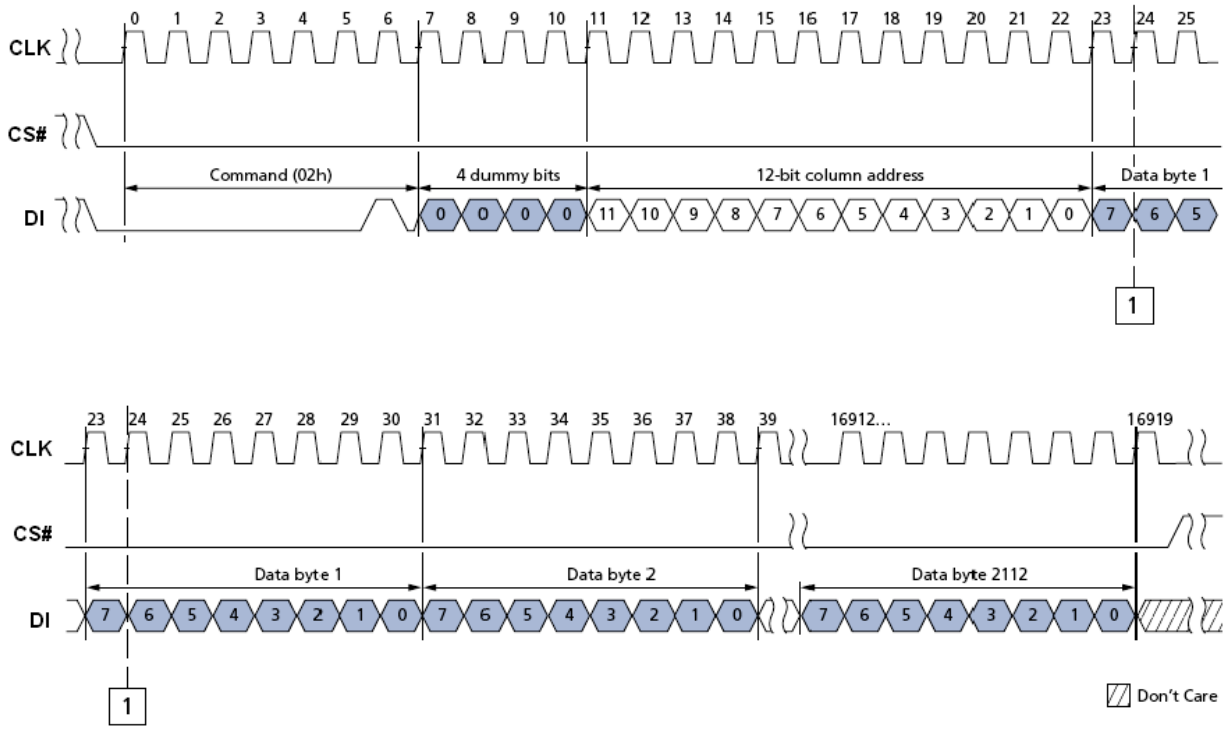


Figure 17. PROGRAM LOAD (02h) Timing

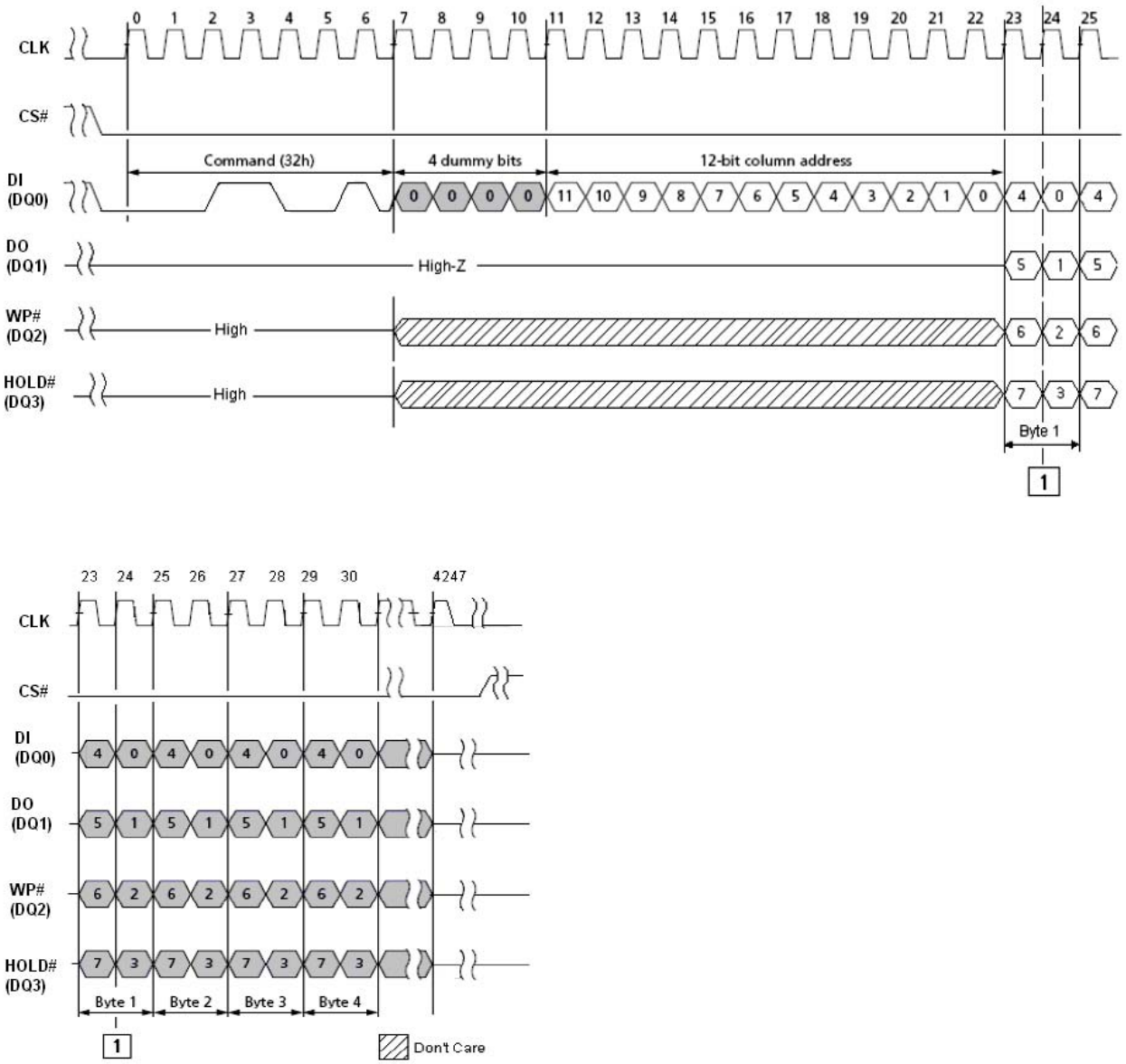


Figure 18. PROGRAM LOAD x4 (32h) Timing

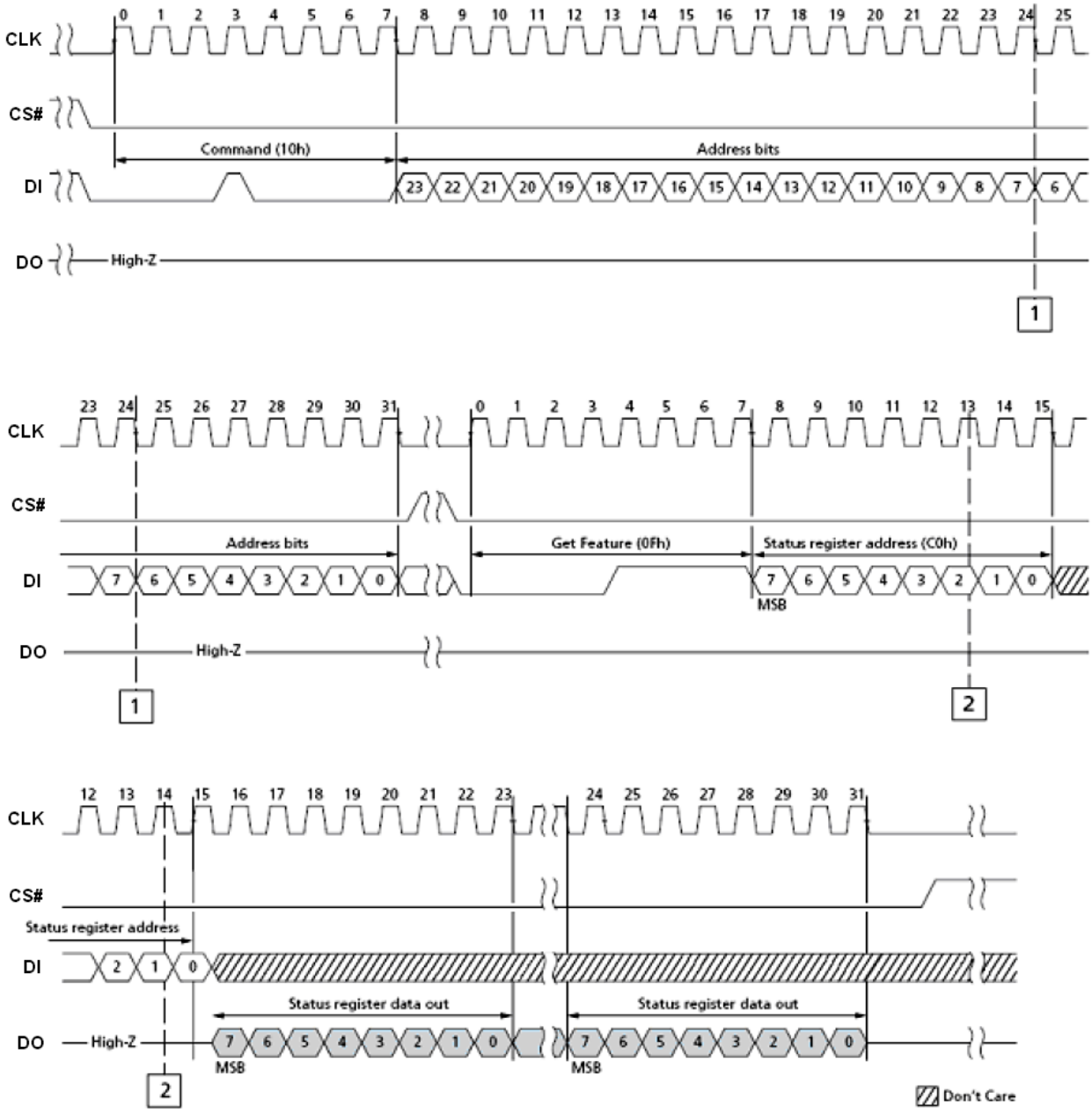


Figure 19. PROGRAM EXECUTE (10h) Timing

Random Data Program

The command sequence is follows:

- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The random data program operation sequence programs data in a page-cache with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

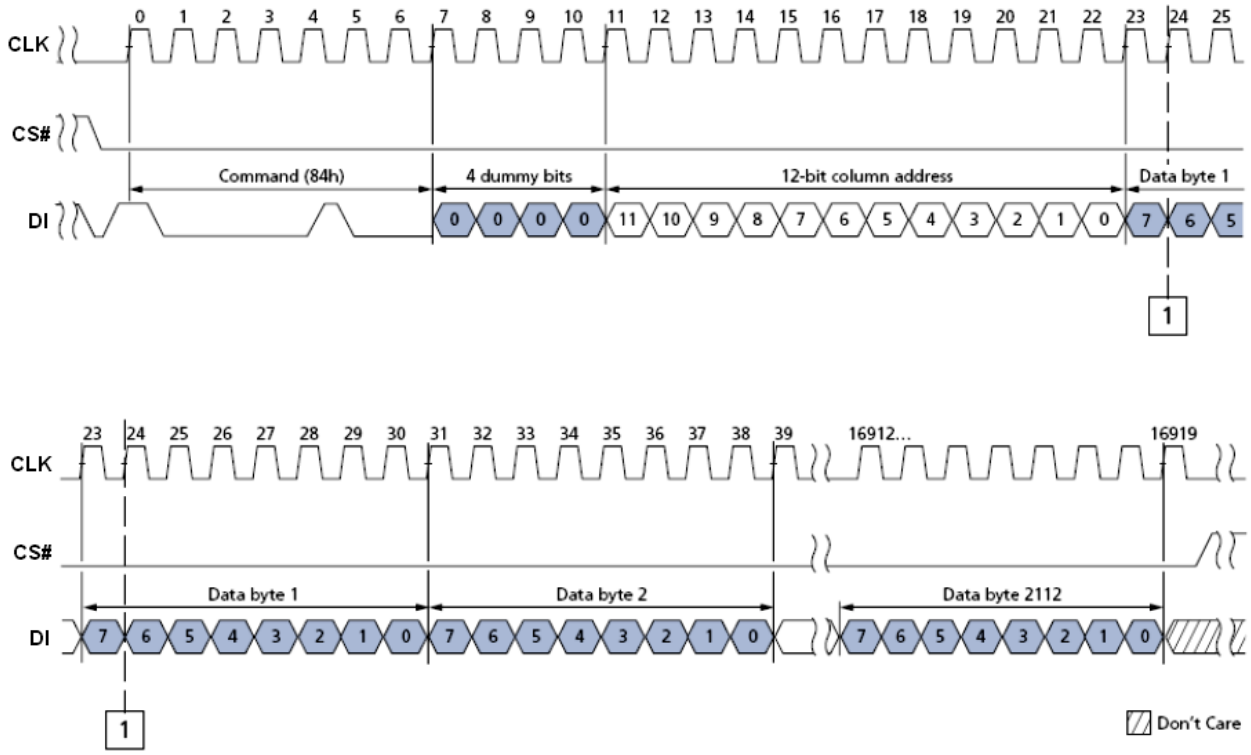


Figure 20. PROGRAM LOAD RANDOM DATA (84h) Timing

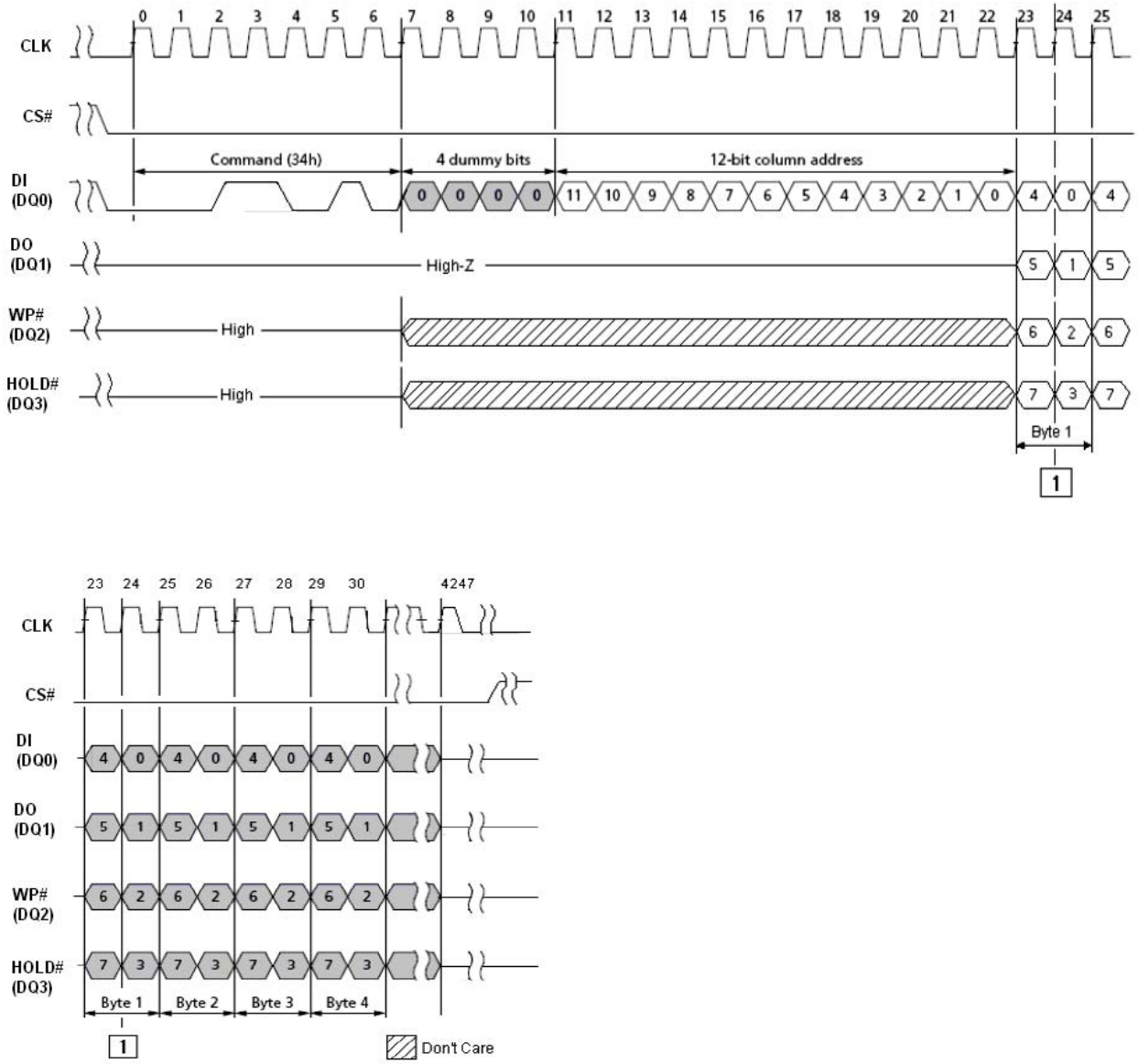


Figure 21. PROGRAM LOAD RANDOM DATA x4 (34h) Timing

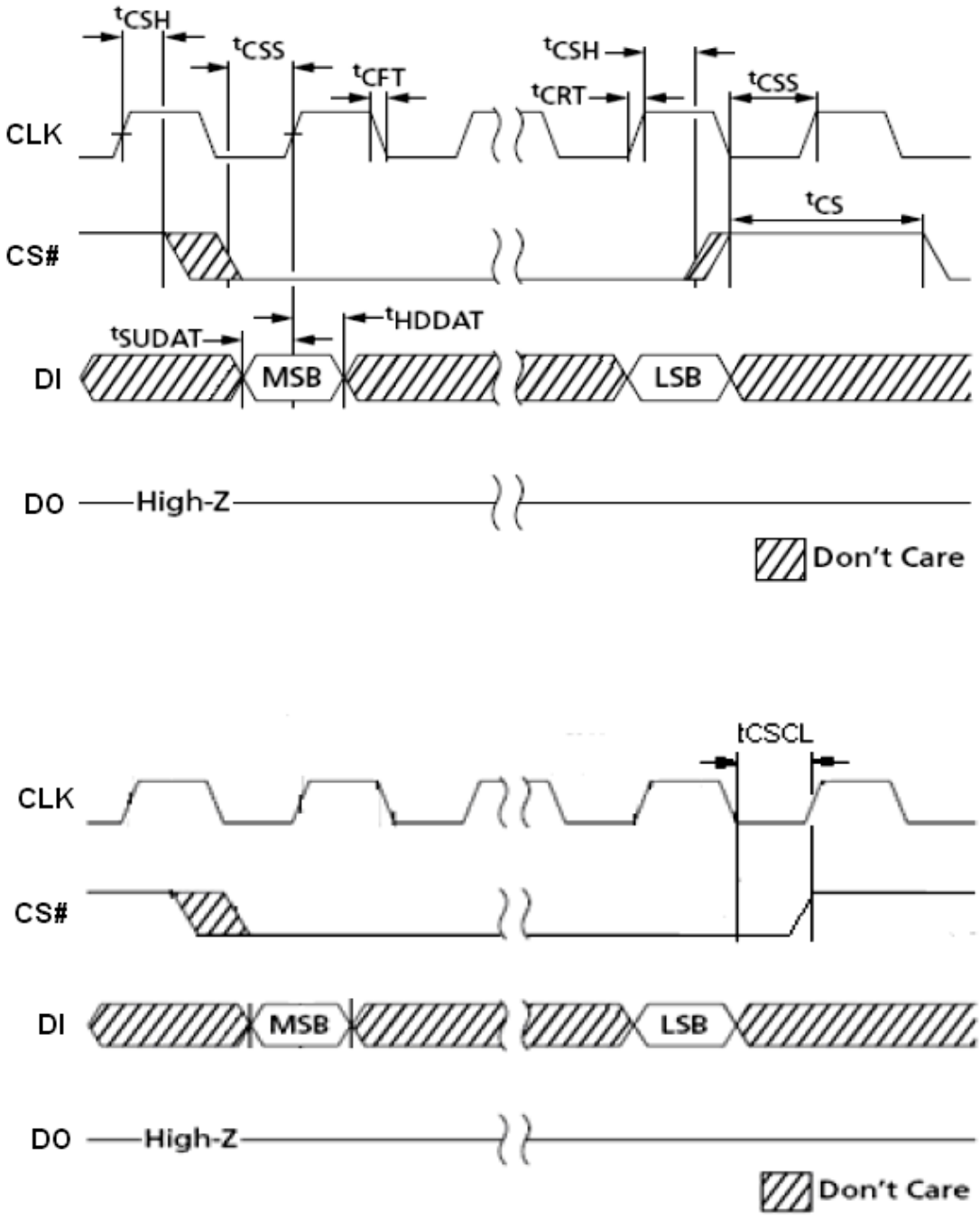


Figure 22. Serial Input and tCSCL Timing

10.3. Internal Data Move

The command sequence is follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4); this is OPTIONAL in sequence.
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence copies or modifies data form page A to page B (Page B should has all FFh data). Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

10.4. Erase Operation

The command sequence is follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 9 dummy bits and a 15-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

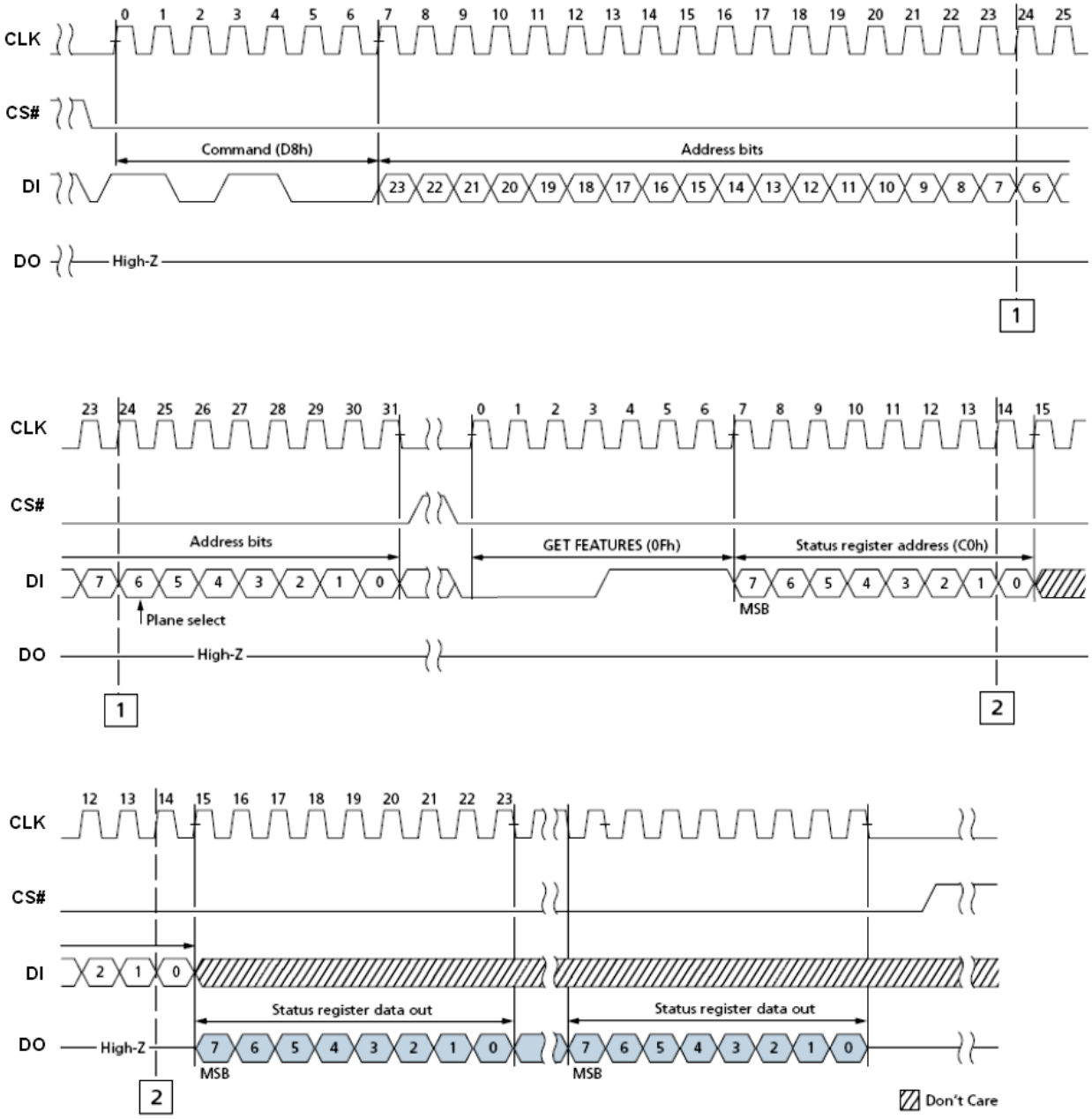


Figure 23. BLOCK ERASE (D8h) Timing

10.5. Read ID

The device contains a product identification mode, initiated by writing 9Fh to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

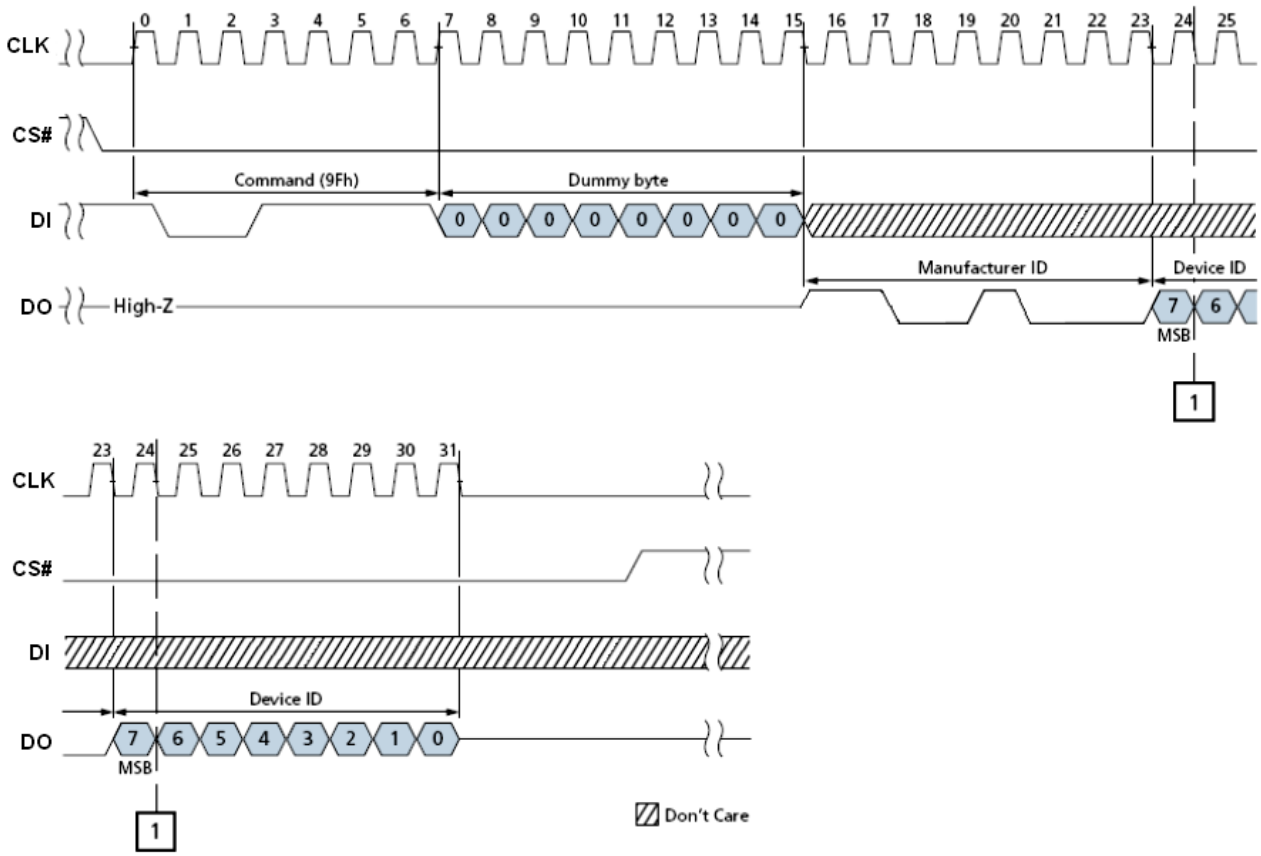


Figure 24. READ ID Timing

Table 11. ID Definition Table

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
EN25LN512	C8h	20h	7Fh	7Fh	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	JEDEC Maker Code Continuation Code, 7Fh
4th Byte	JEDEC Maker Code Continuation Code, 7Fh
5th Byte	JEDEC Maker Code Continuation Code, 7Fh

10.6. WP# Timing

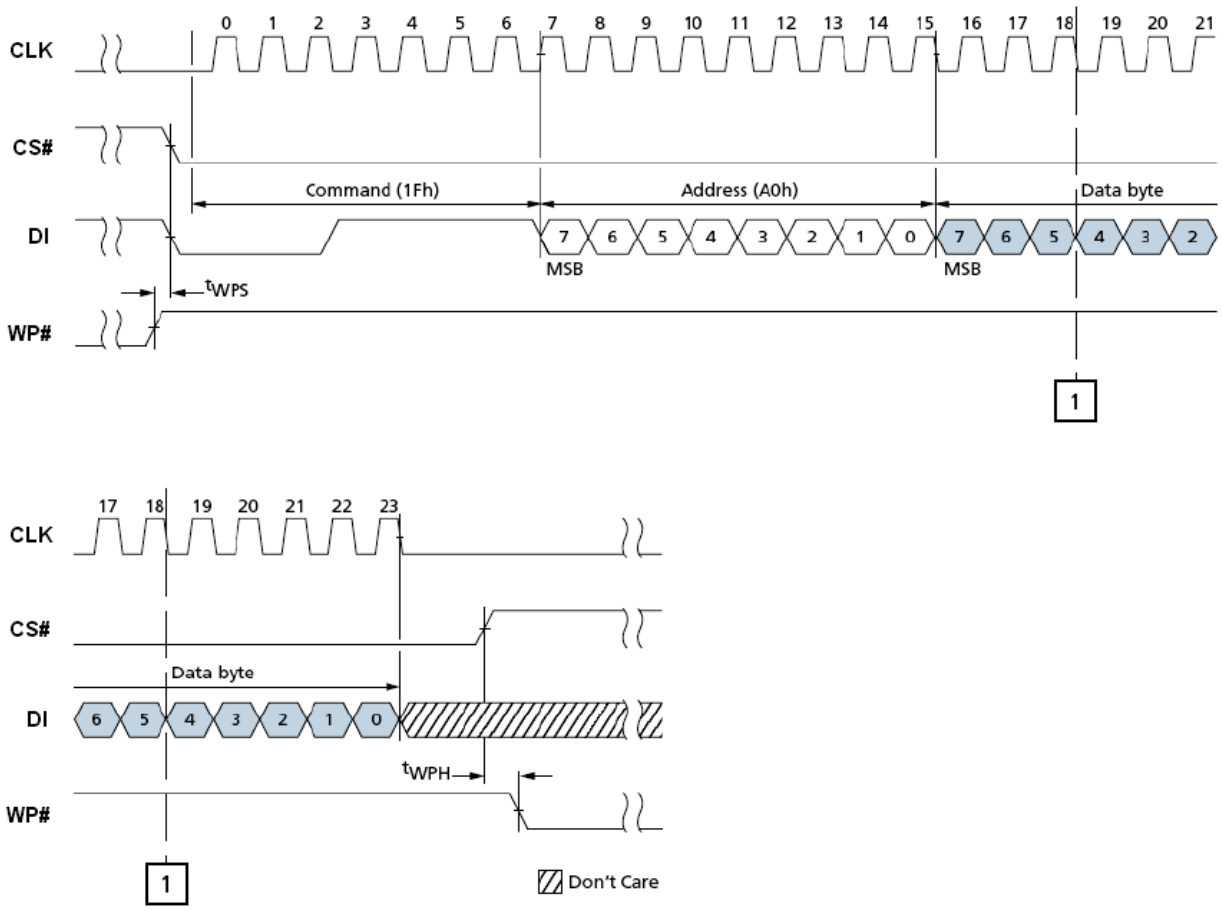


Figure 25. WP# Timing

10.7. HOLD# Timing

HOLD# input provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
Hold mode starts at the falling edge of HOLD# provided CLK is also Low. If CLK is High when HOLD# goes Low, hold mode begins after the next falling edge of CLK. Similarly, hold mode is exited at the rising edge of HOLD# provided CLK is also Low. If CLK is High, hold mode ends after the next falling edge of CLK.
During hold mode, DO is Hi-Z, and DI and CLK inputs are ignored.

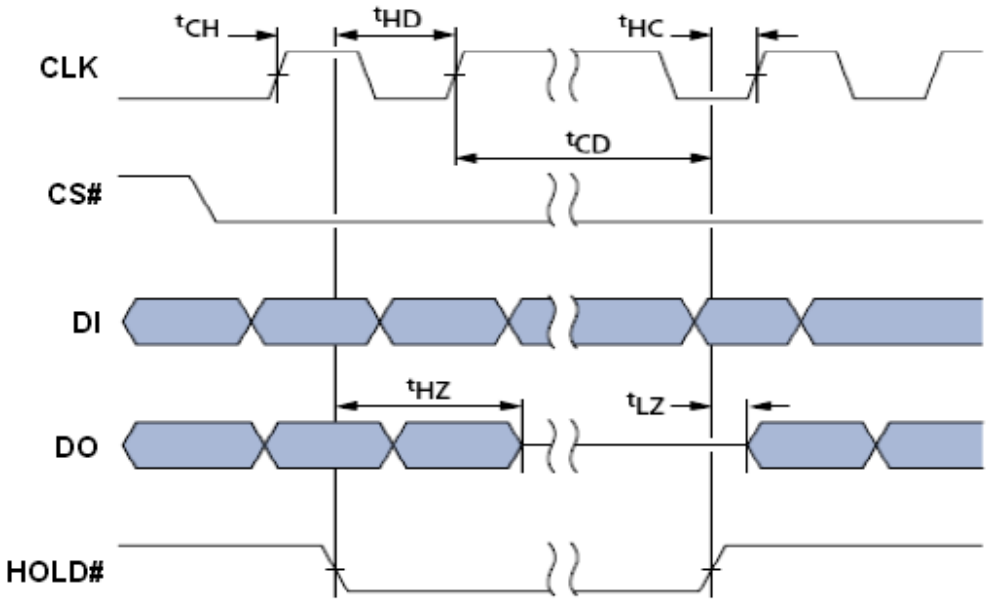


Figure 26. HOLD# Timing

Note:
In high frequency operation, please notice that it may NOT be suitable to pull HOLD# during CLK Low.

10.8. Power-Up

During power transitions, V_{CC} is internally monitored. 250us after V_{CC} has reached 2.5V, WP# is taken High, the device automatically performs the RESET command. The first access to the SPI NAND device can occur 1ms after WP# goes High, and then CS# can be driven Low, CLK can start, and the required command can be issued to the device.

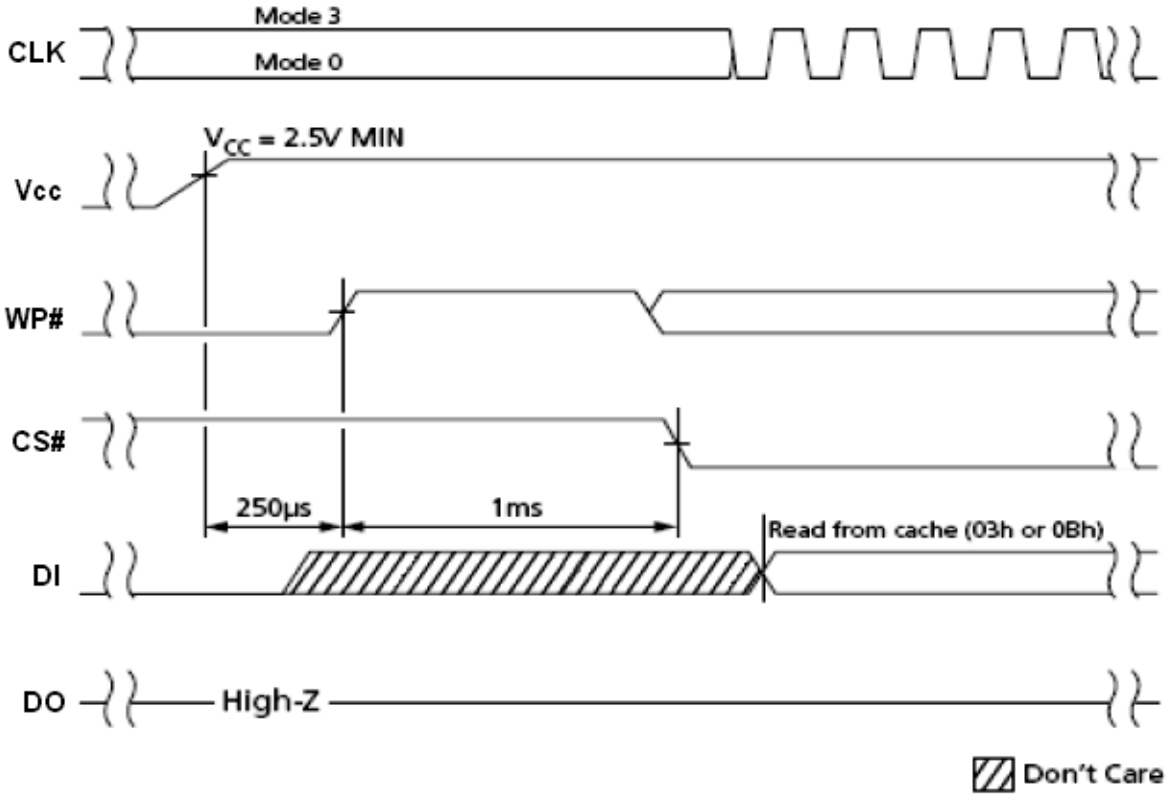


Figure 27. Power-Up and RESET Timing

11. Ordering Information

EN25LN 512 - 104 Y I P

PACKAGING CONTENT
P = RoHS, Halogen-Free and REACH compliant

TEMPERATURE RANGE
I = Industrial (-40℃ to +85℃)

PACKAGE
Y = 8-pin VDFN (6x8mm)
F = 16-pin 300mil SOP

SPEED OPTION for BURST ACCESS TIME
104 = 104MHz

DENSITY
512 = 512 Megabit [(64M + 2M) x 8 Bit]

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25LN = 3.0V Operation SPI-NAND Flash

12. Revisions List

Revision No	Description	Date
A	Initial Release	2013/08/12
B	Supplement the description of One-Time Programmable (OTP) Operations.	2013/09/30
C	Add 16-pin 300mil SOP package option.	2014/02/20