48-Channel Low Voltage High Constant Current LED Driver with 1:4 Time-Multiplexing

Features

Architecture

Quad Flat No-leads

GFN: FN68L

8x8x0.85-0.4

- Support 1~4 multiplexing(scans)
- Support serial peripheral interface (SPI) protocol (Idle is L)
- Support dynamic frame rate: 30Hz~360Hz
- Flexible PWM control to improve visual refresh rate
  - Patented S-PWM technology to improve refresh rate 20KHz
  - Programmable hybrid brightness control
  - Extra 2-bits high luminance mode by zone (I_{OUT}*100%~ I_{OUT}*400%)
- 8-bit adjustable global DC current setting
- Support data gray-scale:
  - PWM: 12bits
  - PAM: 10bits
  - Hybrid: PWM-12bits/PAM-10bits

Constant Current

- 48 constant-current output channels
- Constant output current range per channel:
  - 4~100mA @ 5.0V supply voltage
  - Sustain voltage 24V
- Excellent output current accuracy,
  - Between channels: ±3.0% (Max.) (@25mA & 100mA)
  - Between chips: ±3.0% (Max.) (@25mA & 100mA)

Switching Characteristics

- Maximum data clock frequency: 15MHz @VDD=5.0V
- Maximum built-in grayscale clock frequency:70MHz

6F-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30072, R.O.C.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

Protection Function

- Compulsory LED Open/Short error detection
- Real-time LED Open/Short detection and protection
- Over temperature protection

Other Function

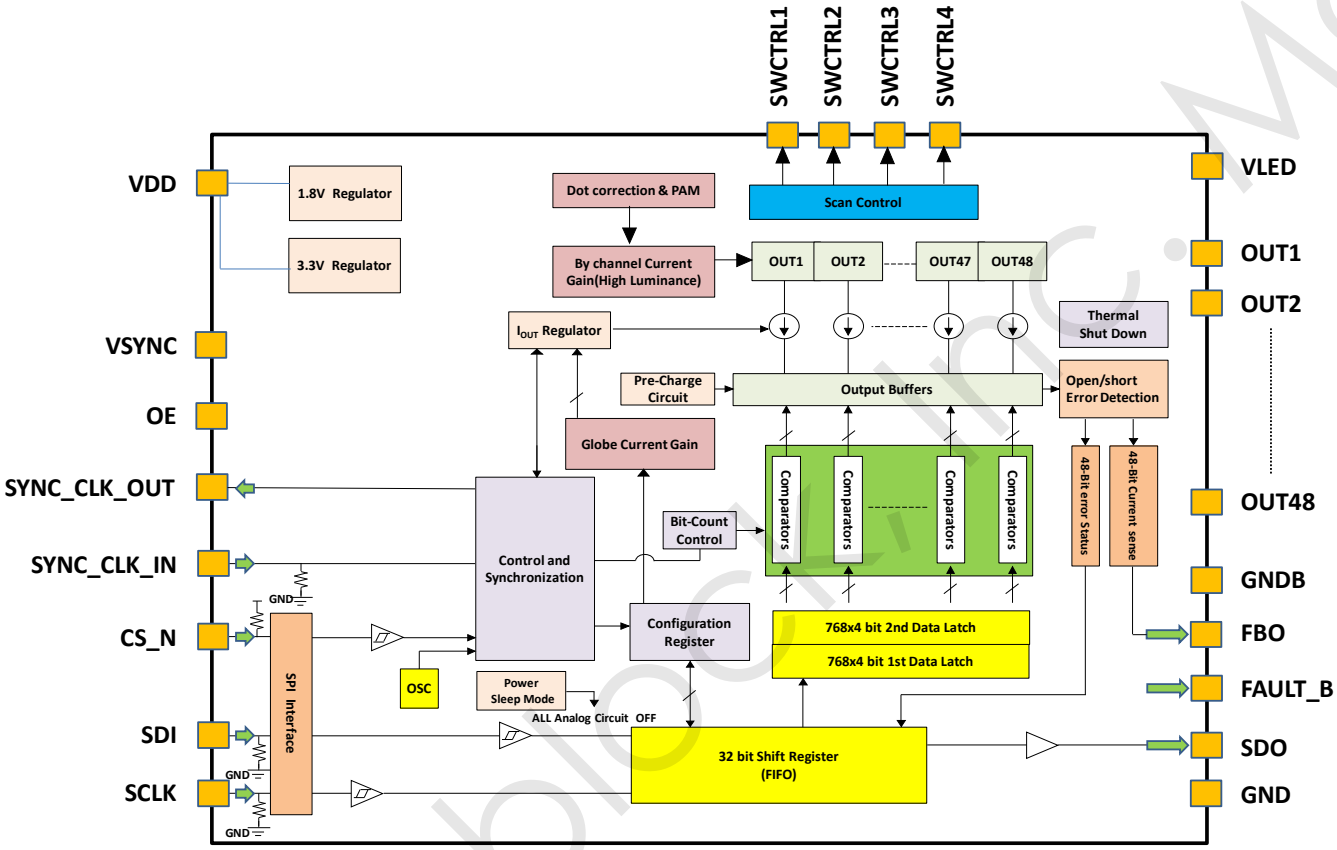
- Frame and scan synchronization for multi-IC application
- Configurable de-ghost function (lower ghost)
- Eliminate dim-line at the first scan
- VSYNC pin for vsync start pulse
- DC-DC converter feedback auto-adjustment function
- Dynamic power saving
- Dynamic black frame insertion
- Individual 3-bit output rising/falling slew rate control
- Support VRR (Variable Refresh Rate)
- Schmitt trigger input
- Package: QFN68 8mm*8mm*0.85mm, pin pitch=0.4mm

Product Description

MBI6353 is an advanced 48-channel high power constant current full-array local dimming (FALD) backlighting LED driver for large-mid LCD panel applications. The innovative architecture is designed to support up to 1:4 time-multiplexing and control up to 192 LED dimming zones application using internal Pulse Width Modulation Dimming(P-DIM) with 12-bit color depth and Analog Dimming(A-DIM) with 10-bit color depth and extra 2-bits high luminance mode by zone to improve contrast ratio for HDR applications.

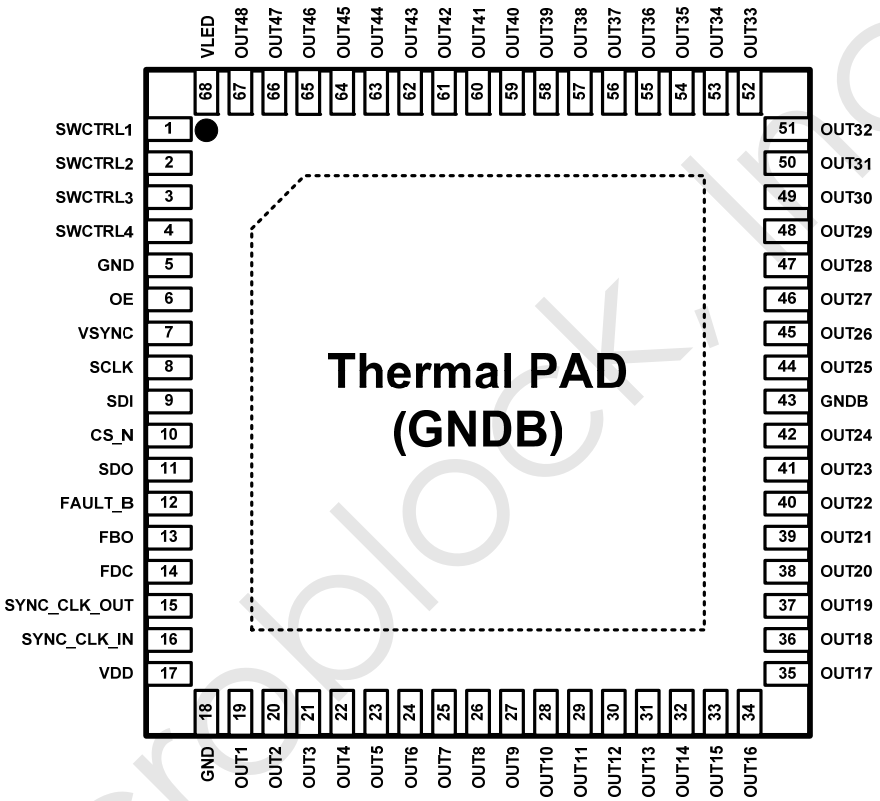
Both compulsory and real-time LED error open/short detection and protection are included during both start-up and normal operation. Besides, MBI6353 also provides DC/DC feedback control, ghost elimination function and over temperature protection features.

Block Diagram



Pin Assignment

- QFN-68L-8x8x0.85-0.4



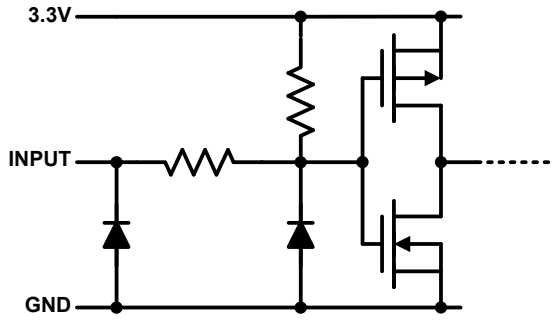
QFN-68-EP (8*8*0.85mm)
(Top View)

Pin Definition

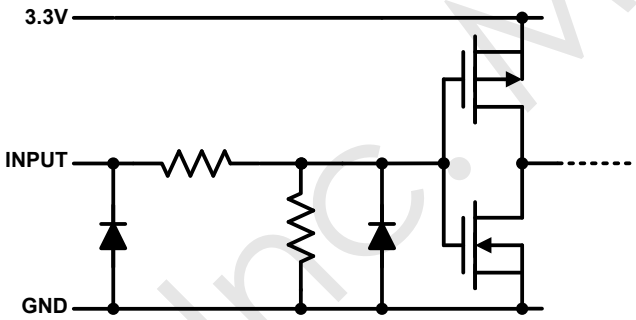
- QFN-68L-8x8x0.85-0.4

No.	Name	Type	Description
1-4	SWCTRL[1:4]	O	Power switch-PMOS gate control. (open drain)
5	GND	-	Analog & digital ground.
6	OE	I	Channel output enable
7	VSYNC	I	Frame data synchronized. (pull-down resistor)
8	SCLK	I	Serial-data clock utilizes for shifting data. (pull-down resistor)
9	SDI	I	Serial-data input to the shift register. (pull-down resistor)
10	CS_N	I	Chip select. (low active) (pull-up resistor)
11	SDO	O	Serial-data output from the shift register. (3.3V)
12	FAULT_B	O	Real-time error status monitor. (open drain) (Error status = over temperature/LED open/LED short)
13	FBO	O	DC-DC Boost converter voltage feedback adjustment. (open drain)
14	FDC	I/O	FBO function communication between ICs. (open drain)
15	SYNC_CLK_OUT	O	Clock synchronized to slave IC. (3.3V)
16	SYNC_CLK_IN	I	Clock synchronized from master IC.
17	VDD	-	Power supply for analog & digital circuit.
18	GND	-	Analog & digital ground.
19-42	OUT1~OUT24	O	Constant current output for LED.
43	GNDB	-	Constant current ground.
44~67	OUT25~OUT48	O	Constant current output for LED.
68	VLED	-	Power supply for driver-specified circuit.
-	Thermal PAD	-	Constant current ground. (The thermal pad must be soldered to ground on PCB.)

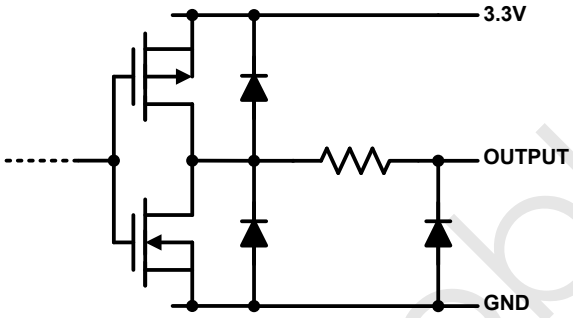
Equivalent Circuits of Inputs and Outputs



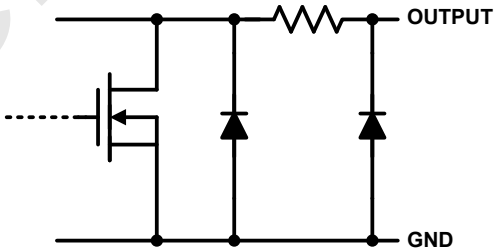
INPUT: CS_N



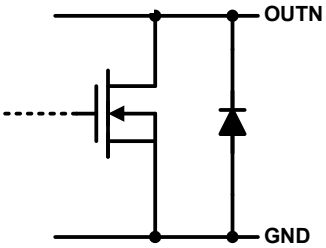
INPUT: SDI, SCLK, VSYNC, OE, FDC, SYNC_CLK_IN



OUTPUT: SDO, SYNC_CLK_OUT



OUTPUT: FBO, FDC, FAULT_B, SWCTRL1~4



OUTPUT: OUT1~OUT48

Absolute Maximum Ratings

Characteristic		Symbol	Rating	Unit
VLED Voltage		V_{LED}	0~26	V
Supply Voltage		V_{DD}	0~5.5	V
Input Voltage		V_{IN}	0~5.5	V
Output Current per Output Channel		I_{OUT}	0~100	mA
Sustaining Voltage at current output port (OUT1~48)		$V_{OUT[n]}$	0~26	V
Sustaining Voltage at scan control port (SWCTRL[1:4])		$V_{SWCTRL[n]}$	0~26	V
Sustaining Voltage at open drain port (FBO/FDC/FAULT_B)		V_{FBO}	0~5.5	V
Sustaining Voltage at data output port (SDO/SYNC_VS_OUT)		$V_{SWCTRL[n]}$	0~5.5	V
GND Terminal Current		I_{GND}	4800	mA
Power Dissipation	QFN-68	P_D	5.00	W
Thermal Resistance	QFN-68	$R_{th(j-a)}$	25.01	°C/W
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C

ESD Ratings

Characteristic	Symbol	Rating	Unit
Human-body model (HBM)*	VESD_HBM	±4500	V
Charged-device model (CDM)*	VESD_CDM	±1000	V

*JESD22-C101

Electrical Characteristics

The following specifications apply for V_{DD}=5V, T_A=25°C, unless otherwise noted.

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
VLED Voltage		V_{LED}	LED anodic voltage	3.2	-	24	V
Supply Voltage		V_{DD}	-	4.5	5	5.5	V
Start Up Voltage		V_{DD_STUP}	-	-	4.3	-	V
UVLO Voltage		V_{DD_UVLO}	-	-	4	-	
Supply Current	Channel ON	$I_{VLED1(ON)}$	GCG1=1/1 GCG2=0(Dec.) (I_{OUT}=25mA) HLM=0, BC=4095(Dec.)	-	0.22	-	mA
		$I_{DD1(ON)}$		-	9.8	-	mA
		$I_{VLED2(ON)}$	GCG1=1/1 GCG2=255(Dec.) (IOUT=100mA) HLM=0, BC=4095(Dec.)	-	0.22	-	mA
		$I_{DD2(ON)}$		-	11.4	-	mA
	Chip Sleep	IVLED(SLPIC)	Chip sleep enable Frame data=0	-	0.02	-	mA
		IDD(SLPIC)		-	3.2	-	mA
Input Logic Voltage*		V_{IH}	SDI/SCLK/VSYNC/OE SYNC_VS_IN/CS_N	2.42	-	VDD	V
		V_{IL}		GND	-	1	V
Output Logic Voltage		V_{OL}	SWCTRL[1:4]/FAULT_B I_{OL}=+2mA	-	-	0.2	V
		V_{OH}	SYNC_VS_OUT/SDO I_{OH}=-2mA	3.1	-	-	V
Input Pull-down Resistor		R_{IN_PD}	SDI/SCLK/VSYNC/OE/FDC/ SYNC_VS_IN	-	580	-	KΩ
Input Pull-up Resistor		R_{IN_PU}	CS_N	-	580	-	KΩ
Output Current		I_{OUT}	OUT1~OUT48=ON V_{OUT}=0.3V~3.0V	4	-	100	mA
		I_{OUT_LEAK}	OUT1~OUT48=OFF V_{OUT}=24V	-	-	1	μA
Current Accuracy	By Channel	dI_{OUT_CH}	GCG1=1/8 GCG2=0(Dec.) (IOUT=3.125mA) HLM=0, BC=4095(Dec.) V_{OUT}=1V	-	-	±4.0	%
			GCG1=1/1 GCG2=0/255(Dec.) (I_{OUT}=25mA/100mA) HLM=0, BC=4095(Dec.) V_{OUT}=1V	-	-	±3.0	%
	By IC	dI_{OUT_IC}	GCG1=1/8 GCG2=0(Dec.) (IOUT=3.125mA) HLM=0, BC=4095(Dec.) V_{OUT}=1V	-	-	±3.0	%
			GCG1=1/1 GCG2=0/255(Dec.) (IOUT=25mA/100mA) HLM=0, BC=4095(Dec.) V_{OUT}=1V	-	-	±3.0	%
Load Regulation (I_{OUT} vs. V_{OUT})		$\%/dV_{OUT}$	GCG1=1/1 GCG2=0/255(Dec.) (I_{OUT}=25mA/100mA) HLM=0, BC=4095(Dec.) V_{DD}=5.0V, V_{OUT}=0.6V/1.0V	-	±0.1	±0.6	% / V

Line Regulation (I_{OUT} vs. V_{DD})	%/dV_{DD}	GCG1=1/1 GCG2=0/255(Dec.) (I_{OUT}=25mA/100mA) HLM=0, BC=4095(Dec.) V_{DD}=4.5V/5V/5.5V, V_{OUT}=1.0V	-	±1.0	±2.0	% / V
Over Temperature Protection	T_{SD}	Thermal shutdown threshold	-	150	-	℃
	T_{SD_HYS}	Recovery hysteresis	-	30	-	℃

*There is a LDO to convert VDD to 3.3V for internal operation, so VIH and VIL are all based on the internal 3.3V.

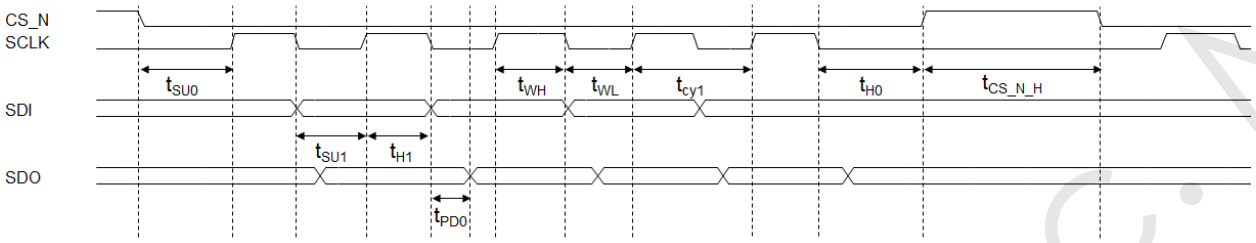
Switching Characteristics

The following specifications apply for V_{DD}=5V, T_A=25°C, unless otherwise noted.

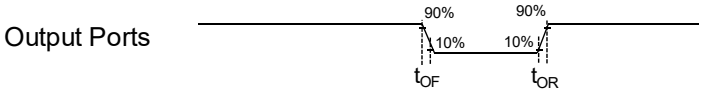
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Cycle time	SCLK clock period	t_{CY1}	IOUT=25mA V_{LED}=24V V_{LOAD}=5V R_L=160Ω C_L=100pF C_1=10uF C_2=0.1μF C_3=10uF C_4=0.1μF C_5=10μF C_6=0.1μF C_{SDO}=50pF		66.67		ns
Data setup Time	CS_N setup time relative to the rise of SCLK	t_{SU0}		33.33	-	-	ns
	SDI setup time relative to the rise of SCLK	t_{SU1}		8	-	-	ns
Data hold Time	CS_N hold time relative to the rise of SCLK	t_{H0}		33.33	-	-	ns
	SDI setup time relative to the rise of SCLK	t_{H1}		8	-	-	ns
	SPI operation relative to the fall of VSYNC	t_{H2}		2	-	-	μs
Pulse Width	High period pulse width of SCLK	t_{WH}		33.33	-	-	ns
	Low period pulse width of SCLK	t_{WL}		33.33	-	-	ns
	High period pulse width of CS_N	$t_{CS\_N\_H}$		2	-	-	μs
	High pulse width of VSYNC	t_{VSYNC}		1	-	-	μs
Compulsory error detection operation time /1scan		t_{ERR-C}		10	-	-	us
Output Rise Time of Output Ports(Highest Speed)		t_{ORH}			100		ns
Output Fall Time of Output Ports(Highest Speed)		t_{OFH}			100		ns
Output Rise Time of Output Ports(Lowest Speed)		t_{ORL}			520		ns
Output Fall Time of Output Ports(Lowest Speed)		t_{OFL}			210		ns

Timing waveform

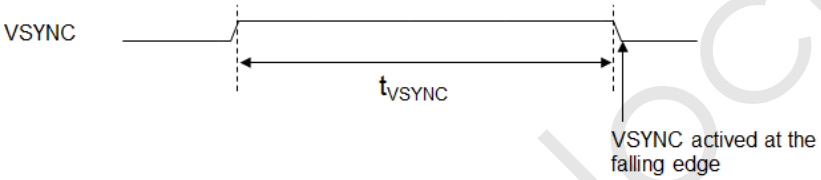
(1)



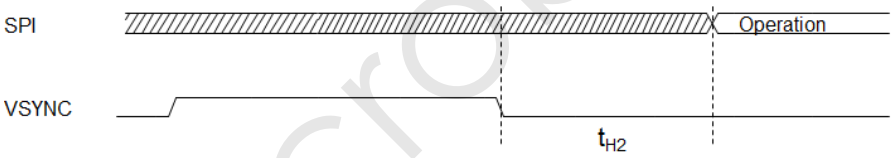
(2)



(3)

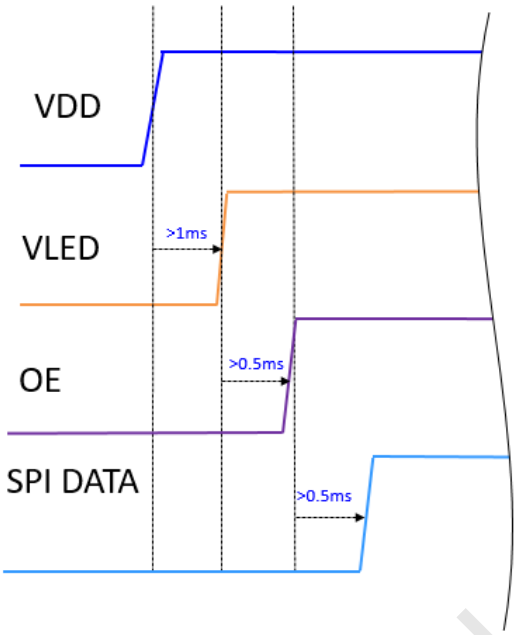


(4)

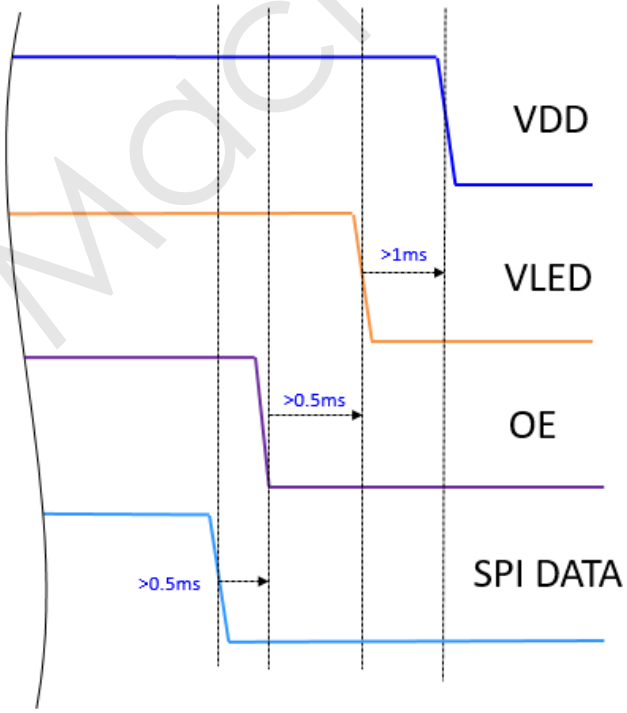


Recommend power-on sequence

- **POWER UP**

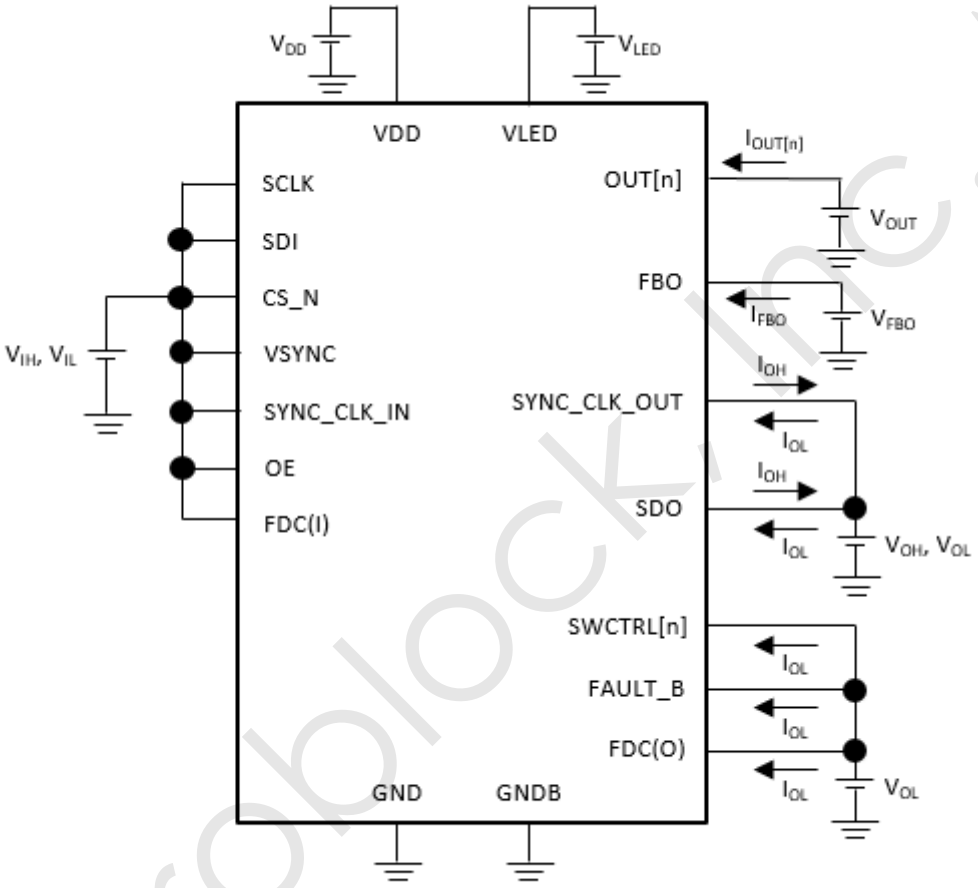


- **POWER DOWN**

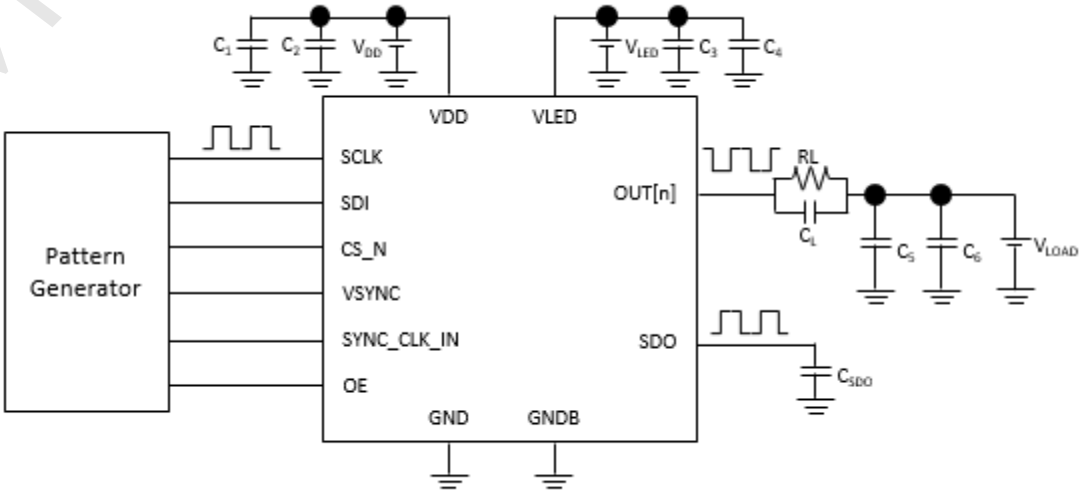


Test Circuit for Electrical/Switching Characteristics

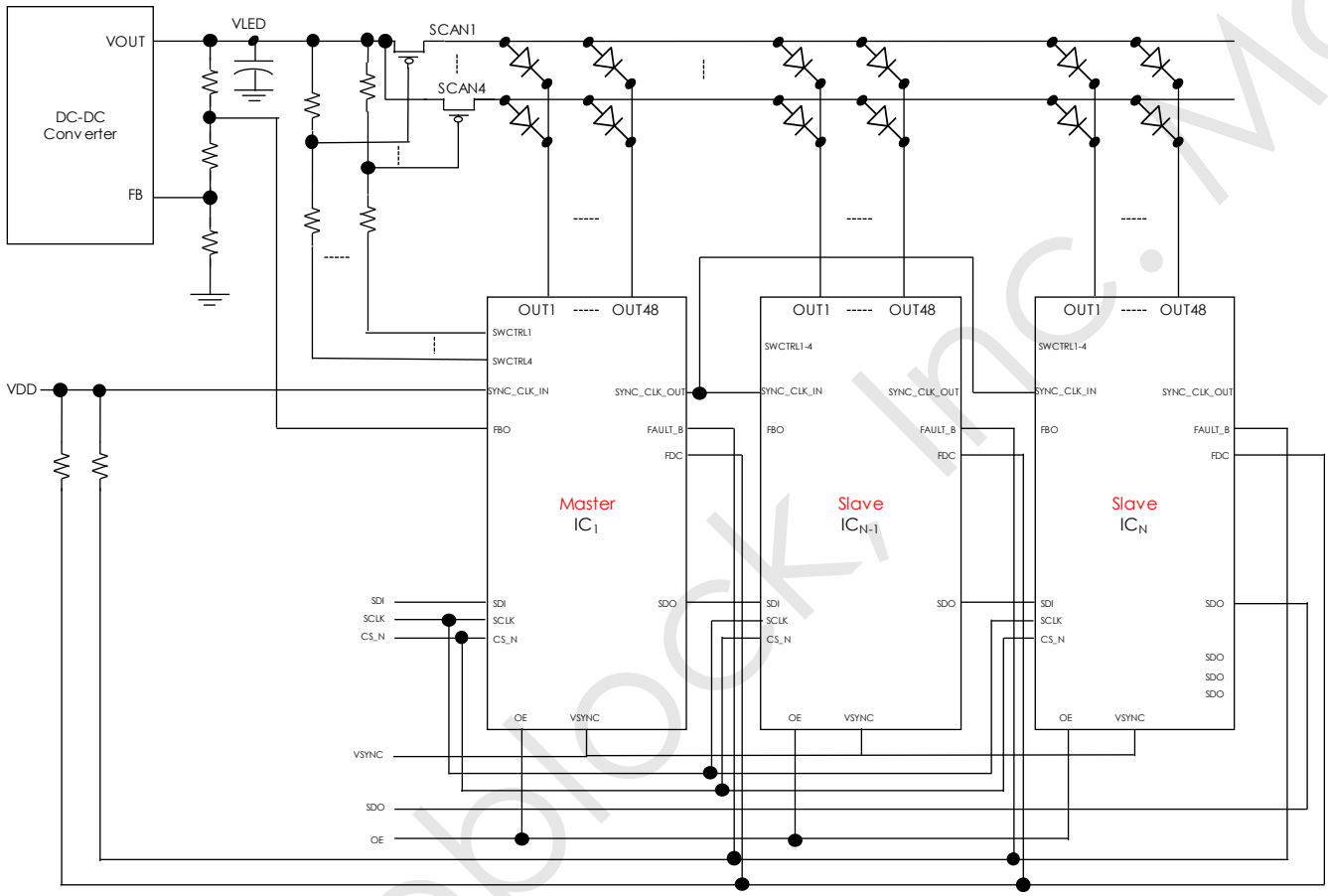
Electrical Characteristics



Switching Characteristics



System application



Output Current Setting

Global output current

The global output current is set by the two configuration registers.

Global output current can be adjusted by “ADDRESS: 0x0, bit 11 ~ bit 10” and “ADDRESS: 0x4, bit 15 ~ bit 8”

SPI ADDRESS:0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
11:10	Read/Write	Global current division (GCG1)	11	Mode change for output current Iout 00: Mode= 1/8 01: Mode= 1/4 10: Mode= 1/2 11: Mode= 1/1

SPI ADDRESS:0x4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GC_7	GC_6	GC_5	GC_4	GC_3	GC_2	GC_1	GC_0	-	-	-	-	-	-	-	-

Bit	Attribute	Definition	Default Value	Function
15:8	Read/Write	Global current setting (GCG2)	00000000	At GCG1=1(Default): 8’b00000000 = 25mA 8’b00000001 = 25.29mA …… 8’b10011001 =70mA …… 8’b11111111 = 100mA

Formula for default setting:

$$I_{OUT} = \left[25 + \left(\frac{GCG2}{255} \times 75\right)\right] \times GCG1 \text{ (Unit: mA)}$$

$$\left[GCG2 = \sum_{n=0}^{7} (GC_n \cdot 2^n) = 0 \sim 255\right]$$

Example:

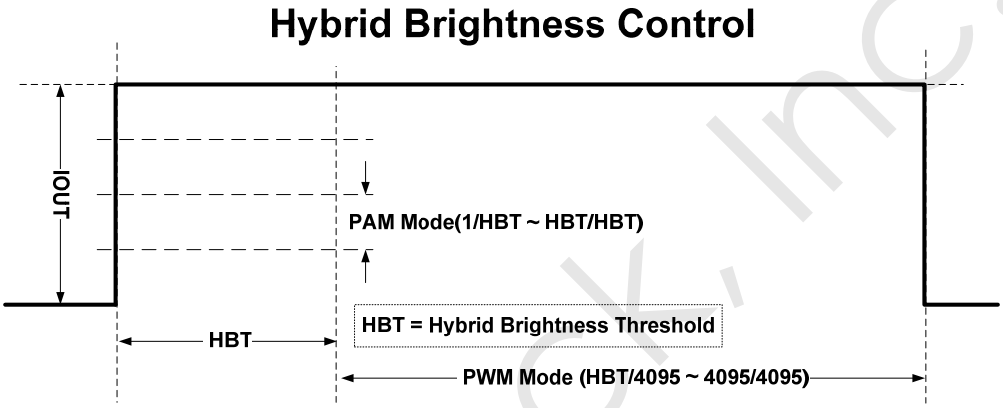
1. GCG1=1/4, GCG2 = 0(default), $I_{OUT} = \left[25 + \left(\frac{0}{255} \times 75\right)\right] \times \frac{1}{4} = 6.25\text{mA}$
2. GCG1=1/2, GCG2 = 85, $I_{OUT} = \left[25 + \left(\frac{85}{255} \times 75\right)\right] \times \frac{1}{2} = 25\text{mA}$
3. GCG1=1(default), GCG2 = 85, $I_{OUT} = \left[25 + \left(\frac{85}{255} \times 75\right)\right] \times 1 = 50\text{mA}$
4. GCG1=1(default), GCG2 = 153, $I_{OUT} = \left[25 + \left(\frac{153}{255} \times 75\right)\right] \times 1 = 70\text{mA}$

Brightness control

Hybrid mode:

There is brightness control with hybrid (PWM/PAM) mode applications in this chip. Configuration register can set brightness mode-change point which is threshold of brightness mode. The brightness code is greater than the threshold using PWM mode, and less than the threshold using PAM mode.

Hybrid mode and PWM only mode are 12-bit brightness control, but PAM only mode is just 10-bit brightness control.



Hybrid (PWM/PAM) brightness threshold can be adjusted by ADDRESS: 0x0, bit 3 ~ bit 0.

SPI ADDRESS:0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	B_{TH3}	B_{TH2}	B_{TH1}	B_{TH0}

Bit	Attribute	Definition	Default Value	Function
3:0	Read/Write	Hybrid(PWM/PAM) brightness threshold	0000	0000: PWM only mode 0001: 4 0010: 8 0011: 16 0100: 32 0101: 64 0110: 128 0111: 256 1000: 512 1001: 1024 1010 ~ 1110: not used(same as code '0000') 1111: PAM only mode (10-bit brightness code only)

High luminance mode:

LED brightness control can be achieved by configuration register of brightness control settings.

Brightness code can be adjusted by ADDRESS: 0x20~0x4F/0x50~0x7F, 0x80~0xAF/0xB0~0xDF, bit 11 ~ bit 0.

High luminance mode can be adjusted by ADDRESS: 0x20~0x4F/0x50~0x7F, 0x80~0xAF/0xB0~0xDF, bit 13 ~ bit 12.

SPI ADDRESS:0x20~0x4F, 0x50~0x7F, 0x80~0xAF, 0xB0~0xDF															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	HL_1	HL_0	BC_{11}	BC_{10}	BC_9	BC_8	BC_7	BC_6	BC_5	BC_4	BC_3	BC_2	BC_1	BC_0

Note:

The register address 0x20~0x4F for SCAN1 Brightness code of Channel48~Channel1 Register

The register address 0x50~0x7F for SCAN2 Brightness code of Channel48~Channel1 Register

The register address 0x80~0xAF for SCAN3 Brightness code of Channel48~Channel1 Register

The register address 0xB0~0xDF for SCAN4 Brightness code of Channel48~Channel1 Register

Formula for default setting:

$$I_{LED\_HYBRID} = [I_{OUT} \times (HLM + 1)] \times \frac{BC\_HYB\_PWM}{HBT} \times \frac{HBT}{4095} \ (Unit: mA)$$

$$I_{LED\_PWM\_only} = [I_{OUT} \times (HLM + 1)] \times \frac{BC\_HYB\_PWM}{4095} \ (Unit: mA)$$

$$I_{LED\_PAM\_only} = [I_{OUT} \times (HLM + 1)] \times \frac{BC\_PAM + 1}{1024} \ (Unit: mA) (Note: I_{LED\_PAM\_only} = 0 \text{ when } BC\_PAM = 0)$$

$$\left[BC\_HYB\_PMW = \sum_{n=0}^{11} (BC_n \cdot 2^n) = 0 \sim 4095\right]$$

$$\left[BC\_PAM = \sum_{n=0}^{9} (BC_n \cdot 2^n) = 0 \sim 1023\right]$$

$$\left[HLM = \sum_{n=0}^{2} (HL_n \cdot 2^n) = 0 \sim 3\right]$$

Digital function

■ Control interface

MBI6353 supports 4-wire SPI interface to communicate with the controller. The communication starts at the CS_N transition from High to Low. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCLK). The protocol consists of 16-bit device address, 16-bit number of data, 16-bit register address and 16-bit data. (Only support SPI mode: CPHA=0 and CPOL=0)

16-bit Device Address

Bit	Definition	Value	Function
15	B	1'b0	Broadcast 1: Message to all device (only write command) 0: Message to single device
14	S	1'b0	Single data 1: Single data transmission (only one word (16 bits) 0: Burst transmission with number of data which is defined by NrOfdata[15:0]
13:8	DevAddr	6'h00~6'h3F	Device Address 0x00: Write/read same data to same register of all devices (B=1) 0x01 to 0x3E: Device address for device 1 to 62 0x3F: Write different data to same register of all devices (B=1)
7:0	Reserved	7'h00	

16-bit Number of Data

Bit	Definition	Value	Function
15:0	NrOfdata	16'h0000~16'hffff	Number of data in frame

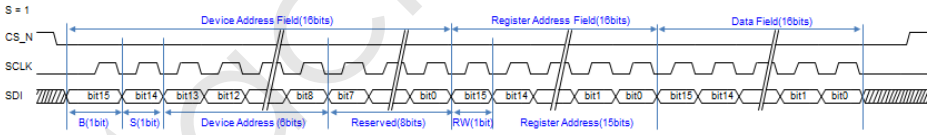
16-bit Register Address

Bit	Definition	Value	Function
15	RW	1'b0	1: Read from register address 0: Write to register address
14:0	RegAddr	15'h0000~15'h7FFF	Register Address

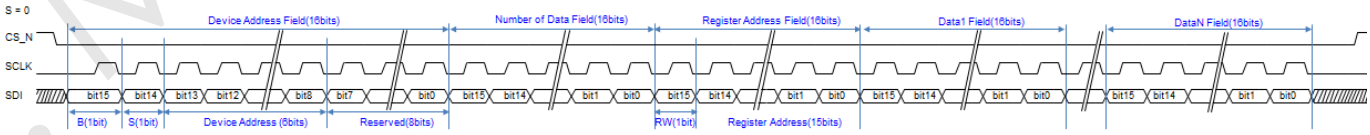
16-bit Data

Bit	Definition	Value	Function
15:0	Data	16'h0000~16'hffff	Data

The single data bit (S) of 16-bit device address is “1”



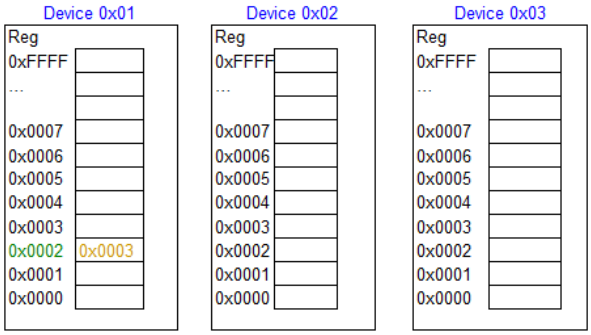
The single data bit (S) of 16-bit device address is “0” (burst mode)

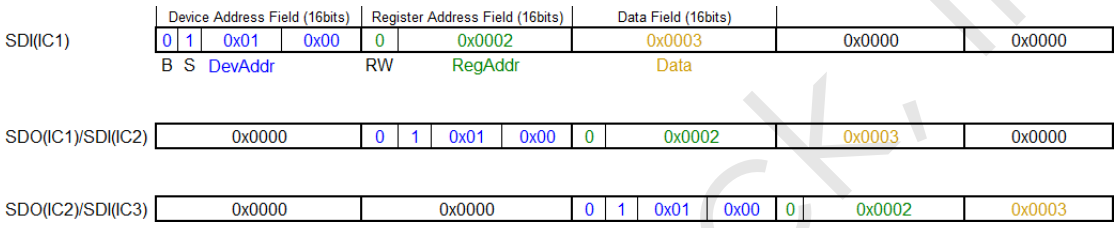


■ Write operation

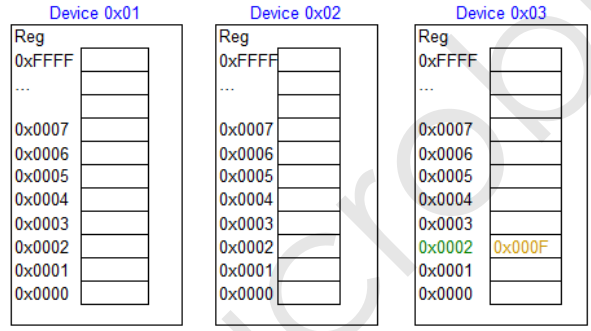
To active the write operation, set the R/W bit to “0”. If the register address of header is set to “N”, the 16-bit data will be written to the register address is “N”

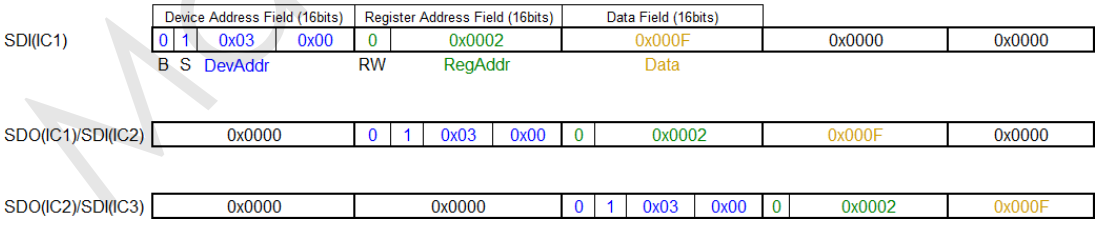
Write single data to device1 when the broadcast bit (B) is set to “0” and single data bit (S) is set to “1”.



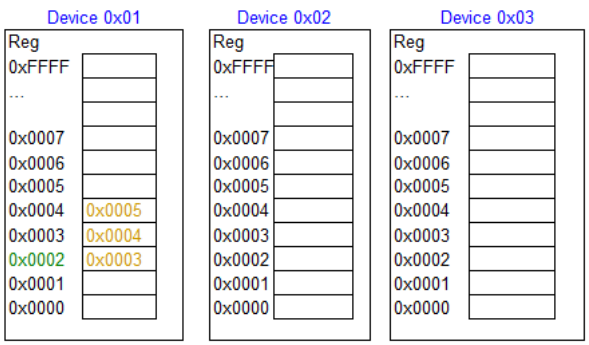


Write single data to device3 when the broadcast bit (B) is set to “0” and single data bit (S) is set to “1”.



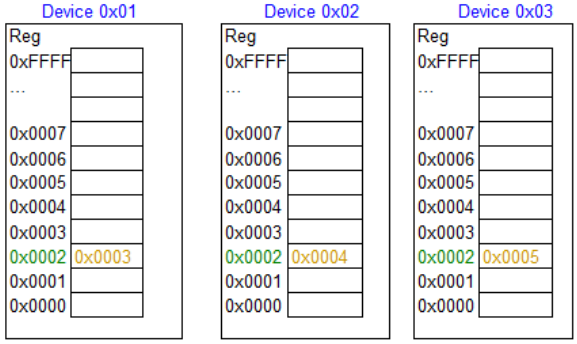


Write multiple data to device1 when the broadcast bit (B) and single data bit (S) are set to “0”.



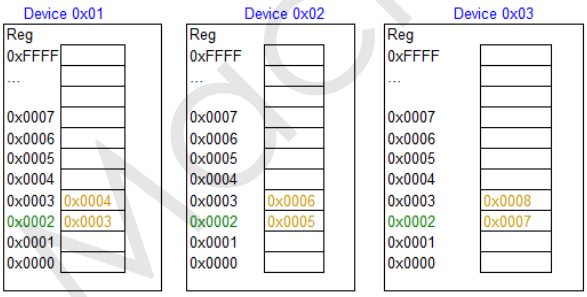
	Device Address Field (16bits)				Number of Data Field (16bits)				Register Address Field (16bits)				Data1 Field (16bits)				Data2 Field (16bits)				Data3 Field (16bits)					
SDI(IC1)	0	0	0x01	0x00	0x0003				0	0x0002			0x0003				0x0004				0x0005				0x0000	0x0000
	B	S	DevAddr		NrOfData				RW	RegAddr			Data1				Data2				Data3					
SDO(IC1)/SDI(IC2)	0x0000				0	0	0x01	0x00	0x0003				0	0x0002			0x0003				0x0004				0x0005	0x0000
SDO(IC2)/SDI(IC3)	0x0000				0x0000				0	0	0x01	0x00	0x0003				0	0x0002			0x0003				0x0004	0x0005

Write different single data to same register address of all device when the broadcast bit (B) and single data bit (S) are set to “1” and the DevAddr bits of 16-bit device address are set to “0x3F”.



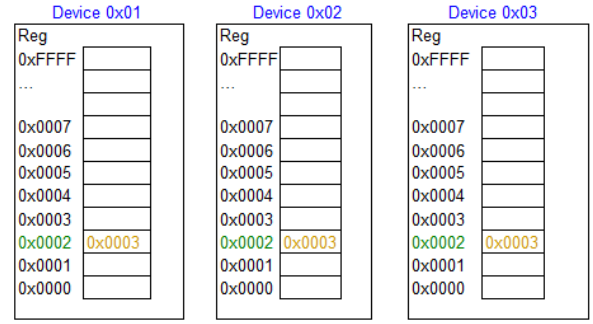
	Device Address Field (16bits)				Register Address Field (16bits)				Data1 Field (16bits)				Data2 Field (16bits)				Data3 Field (16bits)					
SDI(IC1)	1	1	0x3F	0x00	0	0x0002			0x0003				0x0004				0x0005				0x0000	0x0000
	B	S	DevAddr		RW	RegAddr			Data1				Data2				Data3					
SDO(IC1)/SDI(IC2)	0x0000				1	1	0x3F	0x00	0	0x0002			0x0003				0x0004				0x0005	0x0000
SDO(IC2)/SDI(IC3)	0x0000				0x0000				1	1	0x3F	0x00	0	0x0002			0x0003				0x0004	0x0005

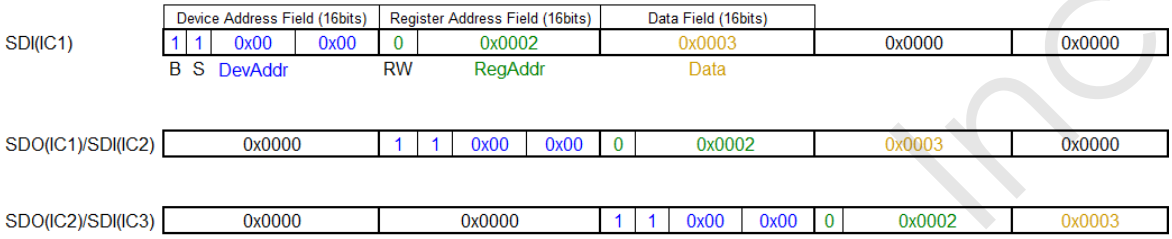
Write different multiple data to all device when the broadcast bit (B) is set to “1”, single data bit (S) is set to “0” and the DevAddr bits of 16-bit device address are set to “0x3F”.



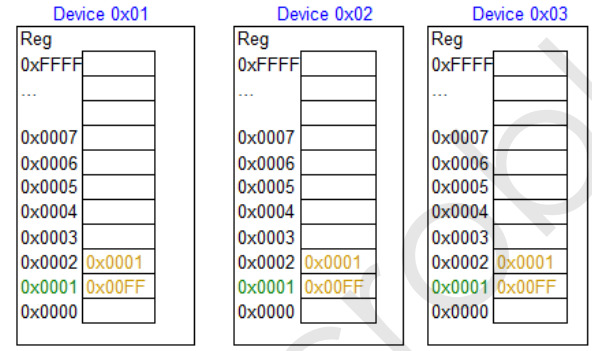
	Device Address Field (16bits)				Number of Data Field (16bits)				Register Address Field (16bits)				Data1 Field (16bits)				Data2 Field (16bits)				Data3 Field (16bits)				Data4 Field (16bits)				Data5 Field (16bits)				Data6 Field (16bits)					
SDI(IC1)	1	0	0x3F	0x00	0x0002				0	0x0002			0x0003				0x0004				0x0005				0x0006				0x0007				0x0008				0x0000	0x0000
	B	S	DevAddr		NrOfData				RW	RegAddr			Data1				Data2				Data3				Data4				Data5				Data6					
SDO(IC1)/SDI(IC2)	0x0000				1	0	0x3F	0x00	0x0002				0	0x0002			0x0003				0x0004				0x0005				0x0006				0x0007				0x0008	0x0000
SDO(IC2)/SDI(IC3)	0x0000				0x0000				1	0	0x3F	0x00	0x0002				0	0x0002			0x0003				0x0004				0x0005				0x0006				0x0007	0x0008

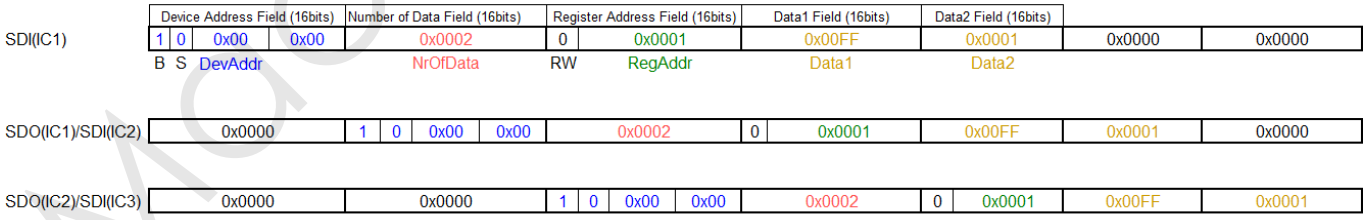
Write same single data to same register address of all device when the broadcast bit (B) and single data bit (S) are set to “1” and the DevAddr bits of 16-bit device address are set to “0x00”.





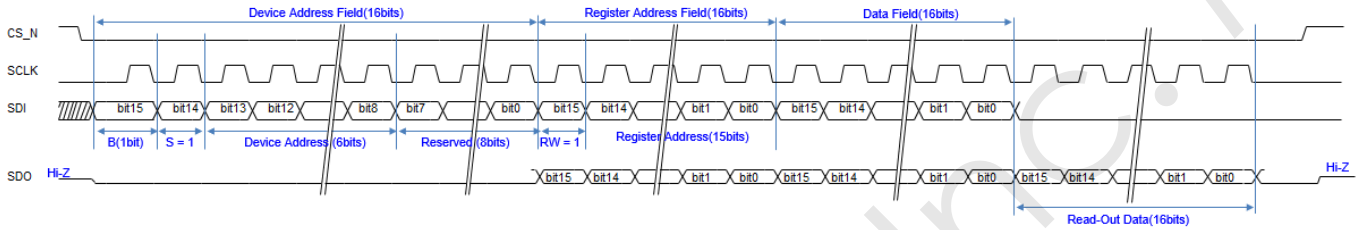
Write multiple same data to same register address of all device when the broadcast bit (B) is set to “1”, single data bit (S) is set to “0” and the DevAddr bits of 16-bit device address are set to “0x00”.



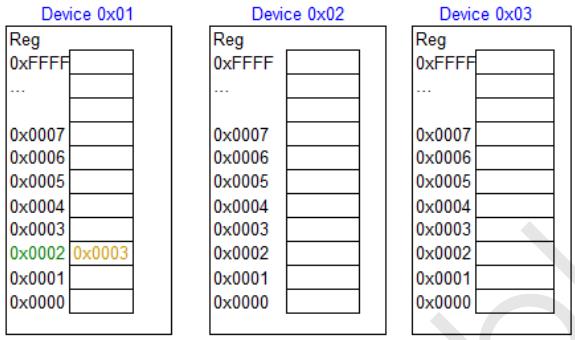


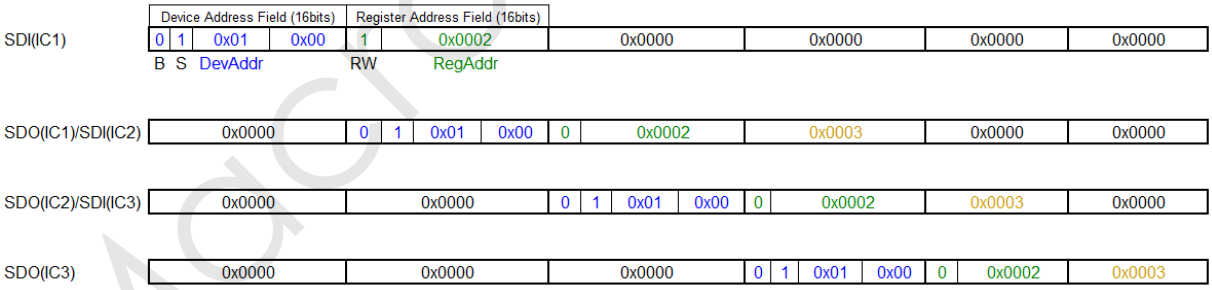
■ Read operation

To active the read operation, set the R/W bit to “1”. If the register address bit is set to “N”, the 16-bit data of register address is “N” will be output by SDO. MBI6353 changes SDO state from high-impedance to output and drives read-out data at the falling edge of SCLK. The read data are transmitted MSB first. After finishing read-out transmission, SDO becomes high-impedance state when CS becomes high. At the read operation, the broadcast (B) bit must keep “0”.



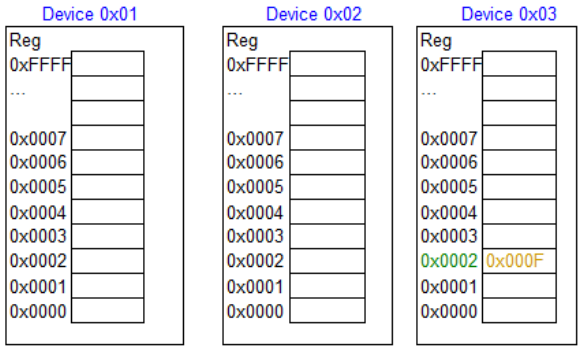
Read single data from device1 when the broadcast bit (B) is set to “0” and single data bit (S) is set to “1”.

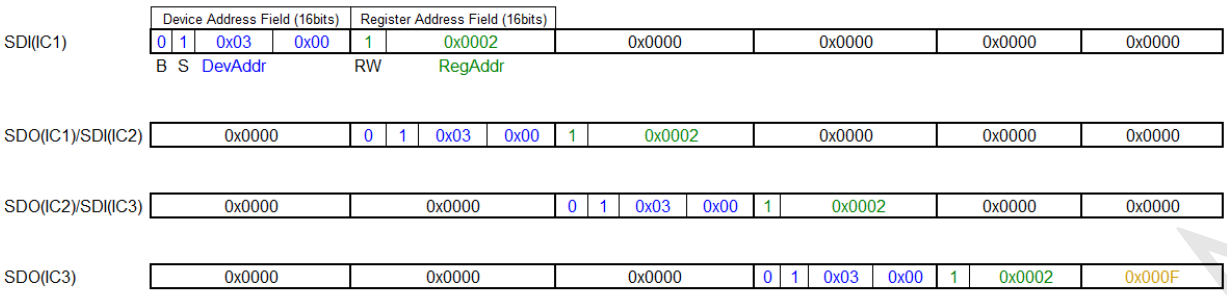




Dummy number(send “0” to SDI(IC1)=(IC number+data number)x16 bits

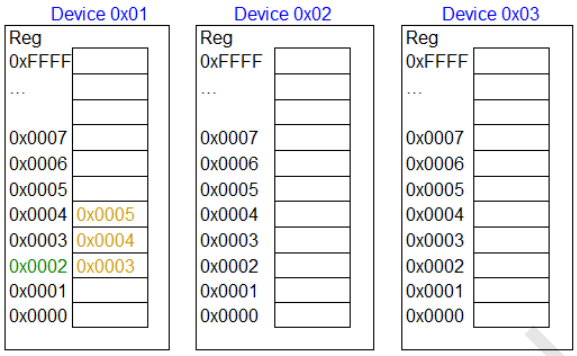
Read single data from device3 when the broadcast bit (B) is set to “0” and single data bit (S) is set to “1”.

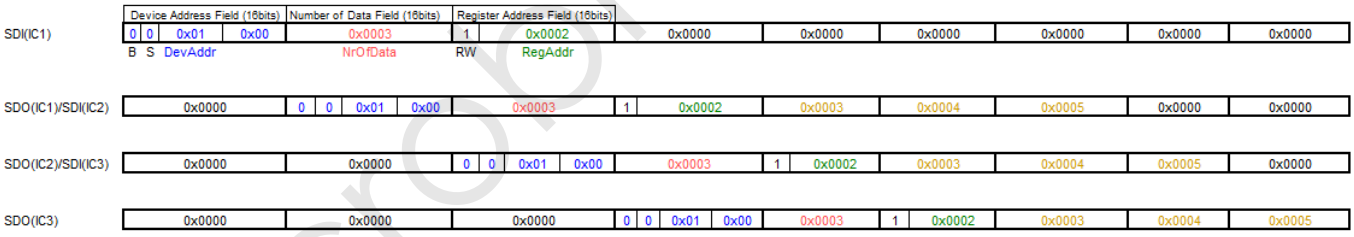




Dummy number(send “0” to SDI(IC1)=(IC number+data number)x16 bits

Read multiple data from device1 when the broadcast bit (B) is set to “0” and single data bit (S) is set to “0”.





Dummy number(send “0” to SDI(IC1)=(IC number+data number)x16 bits

■ SPI Transfer Checksum

MBI6353 supports the interface checksum verification mode. When checksum verification mode is enabled by the bit “checksum” in register 0x01 (bit 0) is set to “1”, the Host controller will add the calculated 16-bit checksum result at the end of SPI transmission.

If the sum of the register address, all data and checksum is zero the transfer is considered as correct. Otherwise the transfer has no effect and the “checksum_fault” bit (Reg. 0x03FF, bit 3) is set until the next valid data transfer.

Checksum calculation Examples:

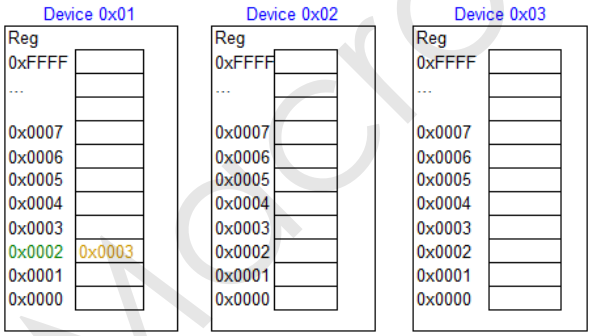
	Device Address Field (16bits)				Number of Data Field (16bits)	Register Address Field (16bits)		Data1 Field (16bits)	Data2 Field (16bits)	Data3 Field (16bits)	Checksum Field (16bits)
SDI(IC1)	0	0	0x01	0x00	0x0003	0	0x0002	0x0003	0x0004	0x0005	0xFFF2
	B	S	DevAddr		NrOfData	RW	RegAddr	Data1	Data2	Data3	Checksum

0002h+0003h+0004h+0005h+FFF2h = 0000h -> checksum result correct

Write operation with checksum enable

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)	CheckSum Field (16bits)		
SDI(IC1)	0	1	0x01	0x00	0	0x0002	0x0003	0xFFFB	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr	Data	Checksum		
SDO(IC1)/SDI(IC2)	0x0000				0	1	0x01	0x00	0	0x0002	0x0003	0xFFFB	0x0000
SDO(IC2)/SDI(IC3)	0x0000				0x0000				0	1	0x01	0x00	0	0x0002	0x0003	0xFFFB	0x0000

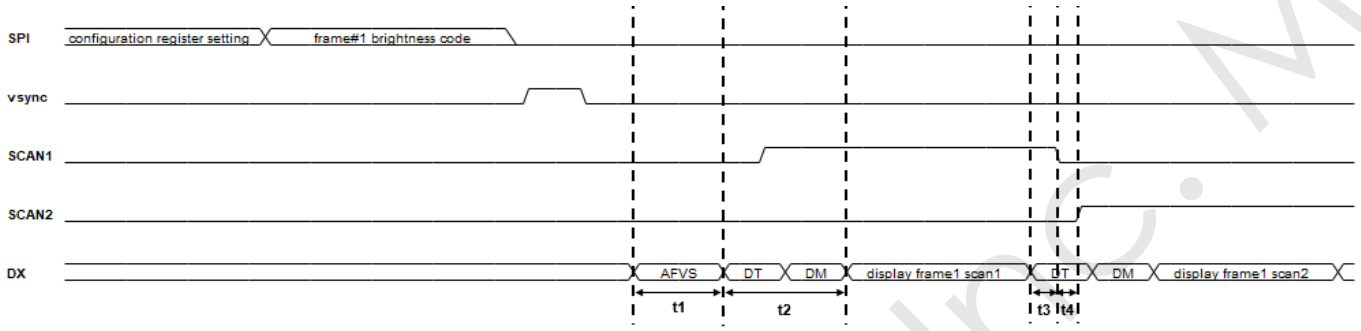
Read operation with checksum enable



	Device Address Field (16bits)				Register Address Field (16bits)		CheckSum Field (16bits)				
SDI(IC1)	0	1	0x01	0x00	1	0x0002	0x7FFE	0x0000	0x0000	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr	Checksum				
SDO(IC1)/SDI(IC2)	0x0000				0	1	0x01	0x00	0	0x0002	0x0003	0x7FFE	0x0000	0x0000
SDO(IC2)/SDI(IC3)	0x0000				0x0000				0	1	0x01	0x00	0	0x0002	0x0003	0x7FFE	0x0000
SDO(IC3)	0x0000				0x0000				0x0000				0	1	0x01	0x00	0	0x0002	0x0003	0x7FFE

■ Initialization Sequence

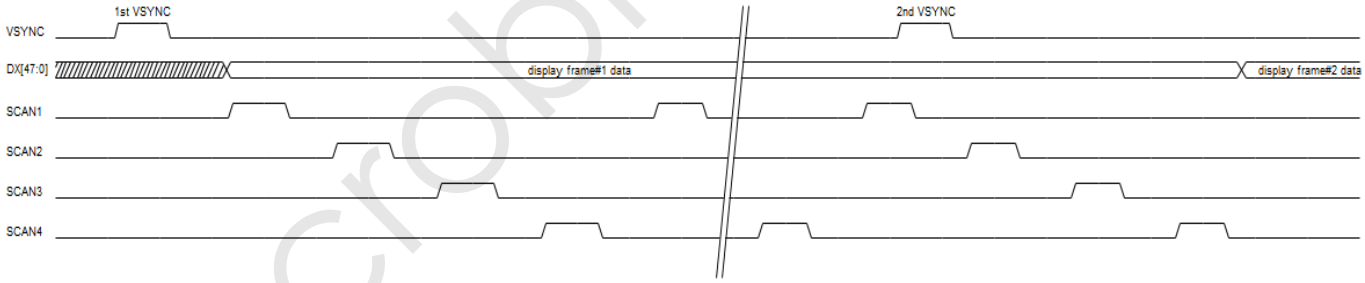
At initialization, users program the configuration register. Then, the send the brightness code register (48 channels x 4 scan lines) and active the “VSYNC” pin. The brightness code will be updated and display by the output channels after the “VSYNC” active.



NOTE:
t1: after vsync period
t2: dead time period(configuration4 register bit[7:0]) + dummy time period(configuration4 register bit[15:8]) GCLK cycles
t3: scan change period(configuration8 register bit[7:0]) GCLK cycles
t4: MOS separate period(configuration8 register bit[15:8]) GCLK cycles

■ Frame data update

The frame1 data will be display by the output channels after the 1st VSYNC active. When the 2nd VSYNC active, the frame2 data will be display by the output channels until the last scan display of the frame1 data is done.



■ Register Lock/Unlock

All registers can be locked to prevent noise from causing the register to be miswritten. Check the status of register lock or unlock by register 0x3FF bit 4.

To unlock write configuration 1~16 (register 0x0~0xF) and channel mask code (register 0x401~0x403) register operation, write data 0xCCXX to register 0x0B00.

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0B00	0xCCXX
	B	S	DevAddr		RW	RegAddr	Data

SDO(IC1)/SDI(IC2)	0x0000		1	1	0x00	0x00	0	0x0B00	0xCCXX			
SDO(IC2)/SDI(IC3)	0x0000		0x0000		1	1	0x00	0x00	0	0x0B00	0xCCXX	

To unlock write brightness code (register 0x20~0xDF) register operation, write data 0xXXAA to register 0x0B00.

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0B00	0xXXAA
	B	S	DevAddr		RW	RegAddr	Data

SDO(IC1)/SDI(IC2)	0x0000		1	1	0x00	0x00	0	0x0B00	0xXXAA			
SDO(IC2)/SDI(IC3)	0x0000		0x0000		1	1	0x00	0x00	0	0x0B00	0xXXAA	

To lock write configuration 1~16 (register 0x0~0xF) and mask code (Register 0x401~0x403) register operation, write data 0xAAXX to register 0x0B00.

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0B00	0xAAXX
	B	S	DevAddr		RW	RegAddr	Data

SDO(IC1)/SDI(IC2)	0x0000		1	1	0x00	0x00	0	0x0B00	0xAAXX			
SDO(IC2)/SDI(IC3)	0x0000		0x0000		1	1	0x00	0x00	0	0x0B00	0xAAXX	

To lock write brightness code (register 0x20~0xDF) register operation, write data 0xXXCC to register 0x0B00.

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0B00	0xXXCC
	B	S	DevAddr		RW	RegAddr	Data

SDO(IC1)/SDI(IC2)	0x0000		1	1	0x00	0x00	0	0x0B00	0xXXCC			
SDO(IC2)/SDI(IC3)	0x0000		0x0000		1	1	0x00	0x00	0	0x0B00	0xXXCC	

■ Compulsory open error detection

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0D00	0x0001
	B	S	DevAddr		RW	RegAddr	Data

■ Compulsory short error detection

	Device Address Field (16bits)				Register Address Field (16bits)		Data Field (16bits)
SDI(IC1)	1	1	0x00	0x00	0	0x0D01	0x0001
	B	S	DevAddr		RW	RegAddr	Data

■ Read open/short error detection result

	Device Address Field (16bits)				Register Address Field (16bits)			
SDI(IC1)	0	1	0x01	0x00	1	0x0D03	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr		

SDO(IC1)	0x0000	0	1	0x01	0x00	1	0x0D03	N

read data from SCAN1 open/short error detection result of Channel48~Channel33)

	Device Address Field (16bits)				Register Address Field (16bits)			
SDI(IC1)	0	1	0x01	0x00	1	0x0D04	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr		

SDO(IC1)	0x0000	0	1	0x01	0x00	1	0x0D04	N

read data from SCAN1 open/short error detection result of Channel32~Channel17)

	Device Address Field (16bits)				Register Address Field (16bits)			
SDI(IC1)	0	1	0x01	0x00	1	0x0D05	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr		

SDO(IC1)	0x0000	0	1	0x01	0x00	1	0x0D05	N

read data from SCAN1 open/short error detection result of Channel16~Channel1)

	Device Address Field (16bits)				Register Address Field (16bits)			
SDI(IC1)	0	1	0x01	0x00	1	0x0D06	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr		

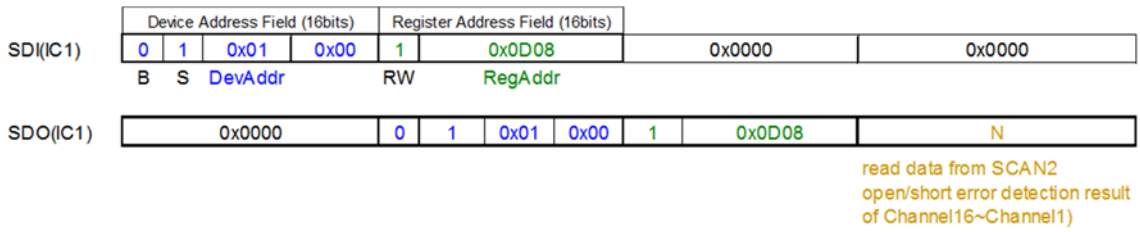
SDO(IC1)	0x0000	0	1	0x01	0x00	1	0x0D06	N

read data from SCAN2 open/short error detection result of Channel48~Channel33)

	Device Address Field (16bits)				Register Address Field (16bits)			
SDI(IC1)	0	1	0x01	0x00	1	0x0D07	0x0000	0x0000
	B	S	DevAddr		RW	RegAddr		

SDO(IC1)	0x0000	0	1	0x01	0x00	1	0x0D07	N

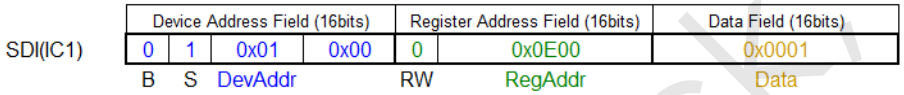
read data from SCAN2 open/short error detection result of Channel32~Channel17)



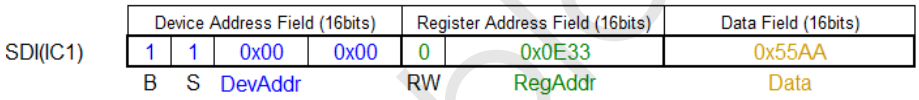
The register 0xD09~0xD0B for the open/short error detection result of SCAN3 of channel48~channel1.

The register 0xD0C~0xD0E for the open/short error detection result of SCAN4 of channel48~channel1.

■ **Software reset command**



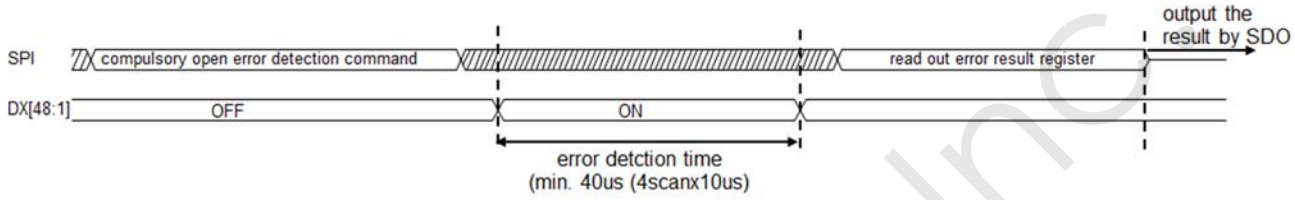
■ **Fault reset command**



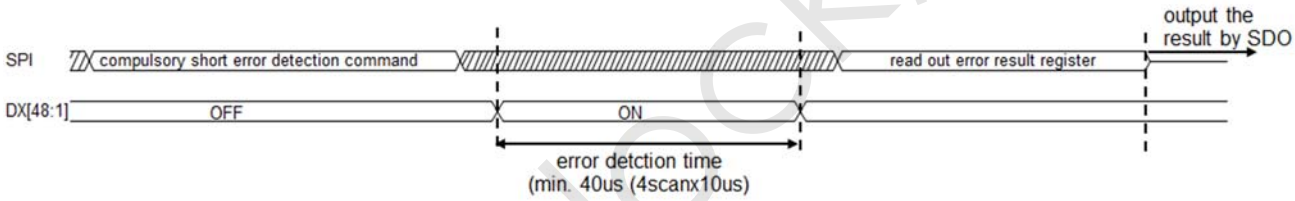
■ Open/Short Error Detection Operation

For the open or short error detection, enable the configuration9 register bit 14 or bit 13. MBI6353 will perform error detection after the “compulsory open/short error detection command”. The result of error detection will be stored on open/short error result (register 0xD03~0xD0E) register after the operation of SCAN1 to SCAN4 is done. The error report will be pushed out after the read out error result register command. MBI6353 shift out MSB of error reports to LSB of error reports from SDO simultaneously.

Compulsory open error detection



Compulsory short error detection



Register Maps

ADDRESS	REGISTER NAME	R/W
0x0	Configuration1 register	R/W
0x1	Configuration2 register	R/W
0x2	Configuration3 register	R/W
0x3	Configuration4 register	R/W
0x4	Configuration5 register	R/W
0x5	Configuration6 register	R/W
0x6	Configuration7 register	R/W
0x7	Configuration8 register	R/W
0x8	Configuration9 register	R/W
0x9	Configuration10 register	R/W
0xA	Configuration11 register	R/W
0xB	Configuration12 register	R/W
0xC	Configuration13 register	R/W
0xD	Configuration14 register	R/W
0xE	Configuration15 register	R
0xF	Configuration16 register	R/W
0x10~0x1F	RESERVE	-
0x20~0x4F	SCAN1 brightness code of Channel48~Channel1	W
0x50~0x7F	SCAN2 brightness code of Channel48~Channel1	W
0x80~0xAF	SCAN3 brightness code of Channel48~Channel1	W
0xB0~0xDF	SCAN4 brightness code of Channel48~Channel1	W
0xE0~0x3FE	RESERVE	-
0x3FF	Fault status register	R
0x401	Channel mask1 code of Channel48~Channel33	R/W
0x402	Channel mask2 code of Channel32~Channel17	R/W
0x403	Channel mask3 code of Channel16~Channel1	R/W
0x404~0xAFF	RESERVE	-
0xB00	Lock/Unlock register	R/W
0xB01~0xCFF	RESERVE	-
0xD00	Compulsory open error detection command	W
0xD01	Compulsory short error detection command	W
0xD03	Open/Short error result register (SCAN1 error detection result of Channel48~Channel33)	R
0xD04	Open/Short error result register (SCAN1 error detection result of Channel32~Channel17)	R
0xD05	Open/Short error result register (SCAN1 error detection result of Channel16~Channel1)	R
0xD06	Open/Short error result register (SCAN2 error detection result of Channel48~Channel33)	R
0xD07	Open/Short error result register (SCAN2 error detection result of Channel32~Channel17)	R
0xD08	Open/Short error result register (SCAN2 error detection result of Channel16~Channel1)	R
0xD09	Open/Short error result register (SCAN3 error detection result of Channel48~Channel33)	R
0xD0A	Open/Short error result register (SCAN3 error detection result of Channel32~Channel17)	R
0xD0B	Open/Short error result register (SCAN3 error detection result of Channel16~Channel1)	R

0xD0C	Open/Short error result register (SCAN4 error detection result of Channel48~Channel33)	R
0XD0D	Open/Short error result register (SCAN4 error detection result of Channel32~Channel17)	R
0xD0E	Open/Short error result register (SCAN4 error detection result of Channel16~Channel1)	R
0xD0F~0xD56	RESERVE	-
0xE00	Software reset command	W
0xE33	Fault reset command	W

Definition of Configuration 1 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:12	Read/Write	RESERVE	0000	-
11:10	Read/Write	Global current division (GCG1)	11	Mode change for output current Iout 00: Mode= 1/8 01: Mode= 1/4 10: Mode= 1/2 11: Mode= 1/1
9:8	Read/Write	Number of scrambles	00	00: 1 scramble 01: 8 scrambles 10: 16 scrambles 11: 32 scrambles
7	Read/Write	RESERVE	0	-
6:5	Read/Write	Number of scans	00	00: 1 scan 01: 2 scans 10: 3 scans 11: 4 scans
4	Read/Write	Display mode	1	0: continue mode, 1: one shot mode
3:0	Read/Write	Hybrid(PWM/PAM) brightness threshold	0000	0000: PWM mode only 0001: 4 0010: 8 0011: 16 0100: 32 0101: 64 0110: 128 0111: 256 1000: 512 1001: 1024 1010 ~ 1110: not used(same as code '0000') 1111: PAM mode only (10-bit brightness code only) **Note:** **If mode change is 2'b00, don't use HBT greater than 128.** **If mode change is 2'b01, don't use HBT greater than 256.** **If mode change is 2'b10, don't use HBT greater than 512.**

Definition of Configuration 2 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0814	-

Definition of Configuration 3 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0019	-

Definition of Configuration 4 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x3															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0xC8C8	-

Definition of Configuration 5 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x4															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:8	Read/Write	Global current setting (GCG2)	00000000	At GCG1=1(Default): 8'b00000000 = 25mA 8'b00000001 = 25.29mA …… 8'b10011001 =70mA …… 8'b11111111 = 100mA
7	Read/Write	RESERVE	0	-
6	Read/Write	HLM function enable	0	0: Disable 1: Enable
5:3	Read/Write	Output channel rising time control (Channel off)	000	000~111 : Low speed to high speed 000: Low speed …… 111:High speed
2:0	Read/Write	Output channel falling time control (Channel on)	000	000~111 : Low speed to high speed 000: Low speed …… 111:High speed

Definition of Configuration 6 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x5															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 7 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x6															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 8 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x7															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 9 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x8															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15	Read/Write	FBO function enable	0	0: Disable 1: Enable
14	Read/Write	Open detection enable	0	0: Disable 1: Enable
13	Read/Write	Short detection enable	0	0: Disable 1: Enable
12:10	Read/Write	Error confirmed number of error detection	111	000: 1 time 001: 2 times 010: 3 times 011: 4 times 100: 5 times 101: 6 times 110: 7 times 111: 8 times
9:8	Read/Write	FBO update period	00	00: 1 frame updated 01: 2 frames updated 10: 3 frames updated 11: 4 frames updated
7	Read/Write	RESERVE	0	-
6	Read/Write	LED error mask enable	1	0: Disable 1: Enable When error counts equal to error confirmed number, mask correspond LED.
5	Read/Write	Interrupt pin enable	1	0: Disable 1: Enable, when error is detected, FAULT_B pin will be pulled low, and it will be recovered to high when error status registers are cleared.
4	Read/Write	RESERVE	0	-
3:2	Read/Write	Open detection voltage	00	00: Level1 01: Level2 10: Level3 11: Level4
1:0	Read/Write	Short detection voltage	00	00: Level1 01: Level2 10: Level3 11: Level4

Definition of Configuration 10 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x9															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 11 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x00FF	-

Definition of Configuration 12 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xB															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0	0	0	0	1	1	0	1	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x181B	-

Definition of Configuration 13 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xC															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 14 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xD															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 15 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	RESERVE	0x0000	-

Definition of Configuration 16 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xF															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:10	Read/Write	RESERVE	000000	-
9	Read/Write	Chip sleep mode enable	0	0: Disable 1: Enable
8:6	Read/Write	RESERVE	0	-
5	Read/Write	Timing reset enable	0	0: Disable 1: Enable, When OE goes low, if the display operation is on going, the display operation will reset to start up state.
4:0	Read/Write	RESERVE	0	-

Definition SCAN1 Brightness code of Channel48~Channel1 Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x20~0x4F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
13:12	Write	HLMS1[1:0]	00	High luminance control 00: IOUT*100% 01: IOUT*200% 10: IOUT*300% 11: IOUT*400% Register address: 0x20, Channel48/SCAN1 high luminance control Register address: 0x21, Channel47/SCAN1 high luminance control Register address: 0x22, Channel46/SCAN1 high luminance control Register address: 0x23, Channel45/SCAN1 high luminance control Register address: 0x24, Channel44/SCAN1 high luminance control Register address: 0x25, Channel43/SCAN1 high luminance control Register address: 0x26, Channel42/SCAN1 high luminance control Register address: 0x27, Channel41/SCAN1 high luminance control Register address: 0x28, Channel40/SCAN1 high luminance control Register address: 0x29, Channel39/SCAN1 high luminance control Register address: 0x2A, Channel38/SCAN1 high luminance control Register address: 0x2B, Channel37/SCAN1 high luminance control Register address: 0x2C, Channel36/SCAN1 high luminance control Register address: 0x2D, Channel35/SCAN1 high luminance control Register address: 0x2E, Channel34/SCAN1 high luminance control Register address: 0x2F, Channel33/SCAN1 high luminance control Register address: 0x30, Channel32/SCAN1 high luminance control Register address: 0x31, Channel31/SCAN1 high luminance control Register address: 0x32, Channel30/SCAN1 high luminance control Register address: 0x33, Channel29/SCAN1 high luminance control Register address: 0x34, Channel28/SCAN1 high luminance control Register address: 0x35, Channel27/SCAN1 high luminance control Register address: 0x36, Channel26/SCAN1 high luminance control

				Register address: 0x37, Channel25/SCAN1 high luminance control Register address: 0x38, Channel24/SCAN1 high luminance control Register address: 0x39, Channel23/SCAN1 high luminance control Register address: 0x3A, Channel22/SCAN1 high luminance control Register address: 0x3B, Channel21/SCAN1 high luminance control Register address: 0x3C, Channel20/SCAN1 high luminance control Register address: 0x3D, Channel19/SCAN1 high luminance control Register address: 0x3E, Channel18/SCAN1 high luminance control Register address: 0x3F, Channel17/SCAN1 high luminance control Register address: 0x40, Channel16/SCAN1 high luminance control Register address: 0x41, Channel15/SCAN1 high luminance control Register address: 0x42, Channel14/SCAN1 high luminance control Register address: 0x43, Channel13/SCAN1 high luminance control Register address: 0x44, Channel12/SCAN1 high luminance control Register address: 0x45, Channel11/SCAN1 high luminance control Register address: 0x46, Channel10/SCAN1 high luminance control Register address: 0x47, Channel9/SCAN1 high luminance control Register address: 0x48, Channel8/SCAN1 high luminance control Register address: 0x49, Channel7/SCAN1 high luminance control Register address: 0x4A, Channel6/SCAN1 high luminance control Register address: 0x4B, Channel5/SCAN1 high luminance control Register address: 0x4C, Channel4/SCAN1 high luminance control Register address: 0x4D, Channel3/SCAN1 high luminance control Register address: 0x4E, Channel2/SCAN1 high luminance control Register address: 0x4F, Channel1/SCAN1 high luminance control

11~0	Write	BCS1[11:0]	000000000000000	Register address: 0x20, Channel48/SCAN1 brightness code Register address: 0x21, Channel47/SCAN1 brightness code Register address: 0x22, Channel46/SCAN1 brightness code Register address: 0x23, Channel45/SCAN1 brightness code Register address: 0x24, Channel44/SCAN1 brightness code Register address: 0x25, Channel43/SCAN1 brightness code Register address: 0x26, Channel42/SCAN1 brightness code Register address: 0x27, Channel41/SCAN1 brightness code Register address: 0x28, Channel40/SCAN1 brightness code Register address: 0x29, Channel39/SCAN1 brightness code Register address: 0x2A, Channel38/SCAN1 brightness code Register address: 0x2B, Channel37/SCAN1 brightness code Register address: 0x2C, Channel36/SCAN1 brightness code Register address: 0x2D, Channel35/SCAN1 brightness code Register address: 0x2E, Channel34/SCAN1 brightness code Register address: 0x2F, Channel33/SCAN1 brightness code Register address: 0x30, Channel32/SCAN1 brightness code Register address: 0x31, Channel31/SCAN1 brightness code Register address: 0x32, Channel30/SCAN1 brightness code Register address: 0x33, Channel29/SCAN1 brightness code Register address: 0x34, Channel28/SCAN1 brightness code Register address: 0x35, Channel27/SCAN1 brightness code Register address: 0x36, Channel26/SCAN1 brightness code Register address: 0x37, Channel25/SCAN1 brightness code Register address: 0x38, Channel24/SCAN1 brightness code Register address: 0x39, Channel23/SCAN1 brightness code Register address: 0x3A, Channel22/SCAN1 brightness code Register address: 0x3B, Channel21/SCAN1 brightness code Register address: 0x3C, Channel20/SCAN1 brightness code Register address: 0x3D, Channel19/SCAN1 brightness code Register address: 0x3E, Channel18/SCAN1 brightness code Register address: 0x3F, Channel17/SCAN1 brightness code

				Register address: 0x40, Channel16/SCAN1 brightness code Register address: 0x41, Channel15/SCAN1 brightness code Register address: 0x42, Channel14/SCAN1 brightness code Register address: 0x43, Channel13/SCAN1 brightness code Register address: 0x44, Channel12/SCAN1 brightness code Register address: 0x45, Channel11/SCAN1 brightness code Register address: 0x46, Channel10/SCAN1 brightness code Register address: 0x47, Channel9/SCAN1 brightness code Register address: 0x48, Channel8/SCAN1 brightness code Register address: 0x49, Channel7/SCAN1 brightness code Register address: 0x4A, Channel6/SCAN1 brightness code Register address: 0x4B, Channel5/SCAN1 brightness code Register address: 0x4C, Channel4/SCAN1 brightness code Register address: 0x4D, Channel3/SCAN1 brightness code Register address: 0x4E, Channel2/SCAN1 brightness code Register address: 0x4F, Channel1/SCAN1 brightness code

Note:

The register address 0x50~0x7F for SCAN2 Brightness code of Channel48~Channel1 Register

The register address 0x80~0xAF for SCAN3 Brightness code of Channel48~Channel1 Register

The register address 0xB0~0xDF for SCAN4 Brightness code of Channel48~Channel1 Register

Definition of Fault status Register

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x3FF															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:5	Read/Write	RESERVE	-	-
4	Read	Register lock/unlock	0	0: register unlock 1: register lock
3	Read	Checksum fault	0	0: normal operation 1: checksum fault
2	Read	LED SHORT fault	0	0: normal operation 1: LED short fault
1	Read	LED OPEN fault	0	0: normal operation 1: LED open fault
0	Read	Thermal Shut-down Detection	0	0: normal operation 1: thermal shut-down triggered

Definition Channel mask0 code of Channel48~Channel33

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x401															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	OUT48~OUT33 mask	0x0000	Channel48~Channel33 mask 0: Normal 1: Mask

Definition Channel mask1 code of Channel32~Channel17

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x402															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	OUT32~OUT17 mask	0x0000	Channel32~Channel17 mask 0: Normal 1: Mask

Definition Channel mask2 code of Channel16~Channel1

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0x403															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Default Value	Function
15:0	Read/Write	OUT16~OUT1 mask	0x0000	Channel16~Channel1 mask 0: Normal 1: Mask

Definition of Open/Short error result (SCAN1 of Channel48~Channel33)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xD03															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read	SCAN1 open/short error detection result of Channel48~Channel33	0xFFFF	Detection result of Channel48~Channel33 0: Error 1: Normal

Definition of Open/Short error result (SCAN1 of Channel32~Channel17)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xD04															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read	SCAN1 open/short error detection result of Channel32~Channel17	0xFFFF	Detection result of Channel32~Channel17 0: Error 1: Normal

Definition of Open/Short error result (SCAN1 of Channel16~Channel1)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

SPI ADDRESS:0xD05															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Default Value	Function
15:0	Read	SCAN1 open/short error detection result of Channel16~Channel1	0xFFFF	Detection result of Channel16~Channel1 0: Error 1: Normal

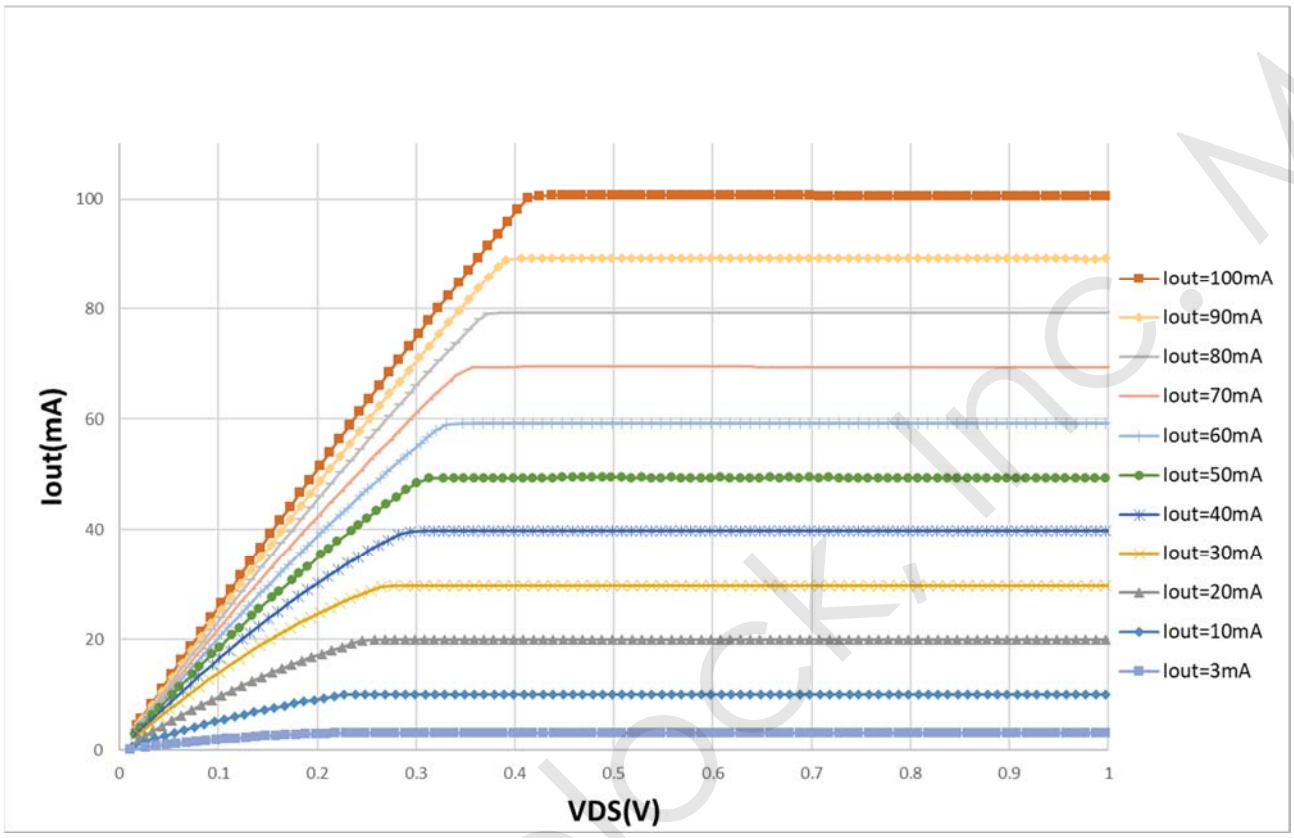
Note:

The register address 0xD06~0xD08 for SCAN2 open/short error detection result of Channel48~Channel1 Register

The register address 0xD09~0xD0B for SCAN3 open/short error detection result of Channel48~Channel1 Register

The register address 0xD0C~0xD0E for SCAN4 open/short error detection result of Channel48~Channel1 Register

I-V curve



Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 48 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x48)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:
$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/48\}$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GFN	25.01	5.00

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

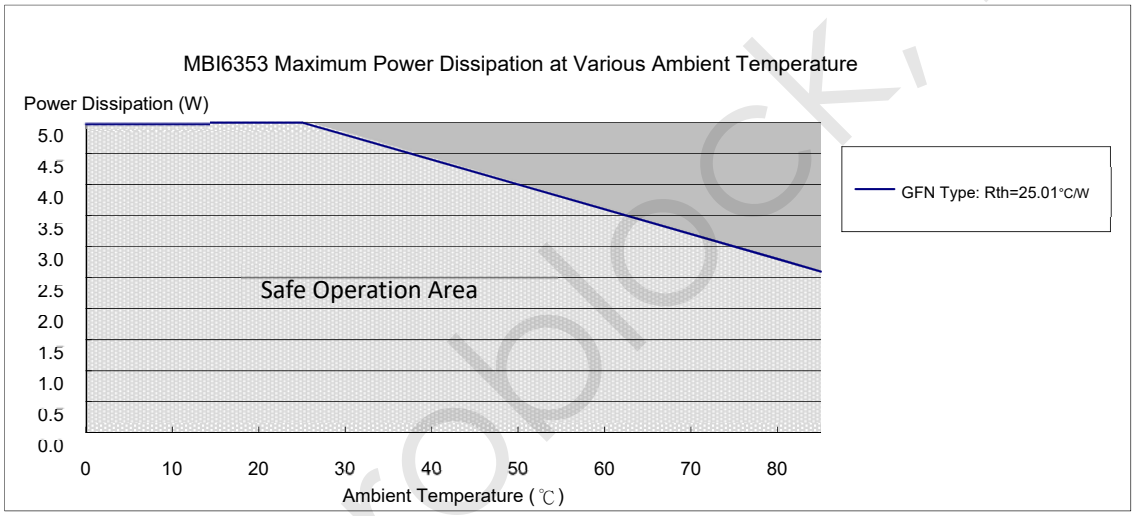
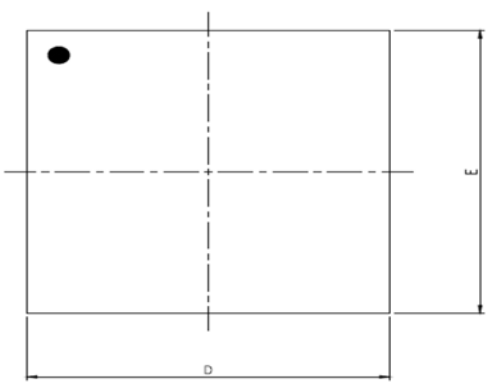
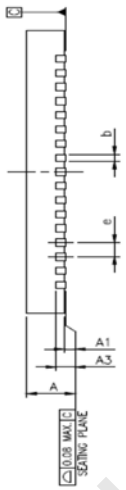


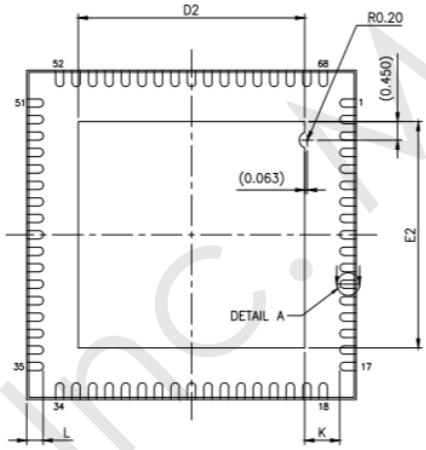
Fig. 6

Package Outline



Top View





Bottom View

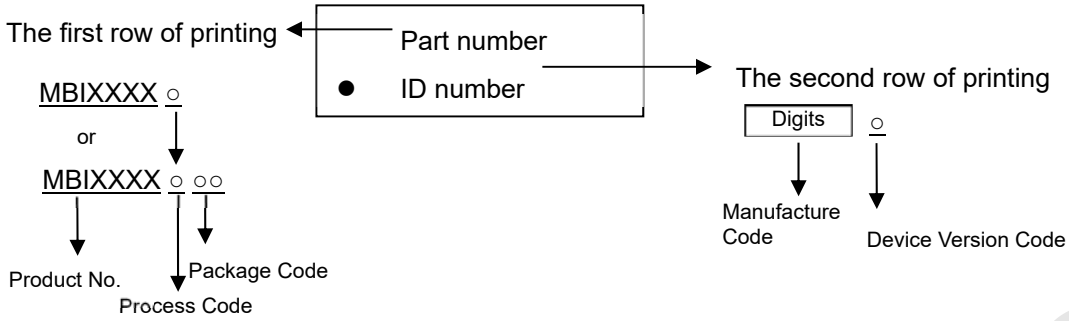
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y8W2)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
236X23* MIL	5.45	5.50	5.55	5.45	5.50	5.55	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

MBI6353GFN Outline Drawing

Product Top Mark Information



Product Revision History

Datasheet Version	Device Version Code
V1.00	A

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI6353GFN-A	QFN68-8*8*0.85-0.4	0.1707

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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