

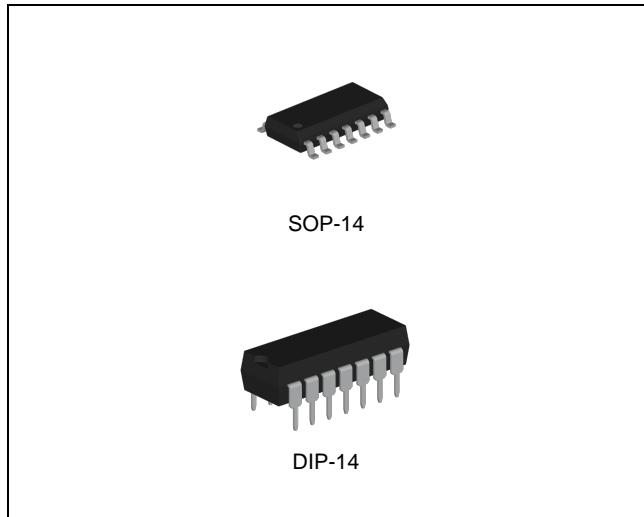
FEATURES

- Wide Operating Voltage Range of 3.0V to 18.0V
- Maximum Input Current of 1 μ A at 18V over Full Package-Temperature range, 100nA at 18V and 25°C
- Standardized Symmetrical Output Characteristics
- Noise Margin
 - 1.0V min @ 5.0V supply
 - 2.0V min @ 10.0V supply
 - 2.5V min @ 15.0V supply

DESCRIPTION

The CD4081B consist of four AND gate circuits. Each circuit functions as a two-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} . Unused inputs must be connected to V_{DD} , V_{SS} , or another input. Unused outputs must be left open.



ORDERING INFORMATION

Device	Package
CD4081BD	SOP-14
CD4081BN	DIP-14

ABSOLUTE MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5	20	V
DC Input Voltage (Referenced to V_{SS})	V_{IN}	-0.5	$V_{DD} + 0.5$	V
DC Input Current	I_{IN}	-	± 10	mA
Maximum Junction Temperature	T_J	-	150	°C
Storage Temperature	T_{STG}	-65	150	°C

Note1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CMOS Quad 2-Input AND Gates

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RECOMMENDED OPERATING CONDITIONS (Note 2)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{DD}	3	18	V
DC Input Voltage	V_{IN}	0	V_{DD}	V
DC Output Voltage	V_{OUT}	0	V_{DD}	V
Operating Free-Air Temperature Range	T_A	-55	125	°C

Note 2. The device is not guaranteed to function outside its operating ratings.

ORDERING INFORMATION

Package	Order No.	Description	Supplied As	Status
SOP-14	CD4081BD	Quad 2-Input AND Gate	Tape & Reel	Active
DIP-14	CD4081BN	Quad 2-Input AND Gate	Tube	Active

CMOS Quad 2-Input AND Gates

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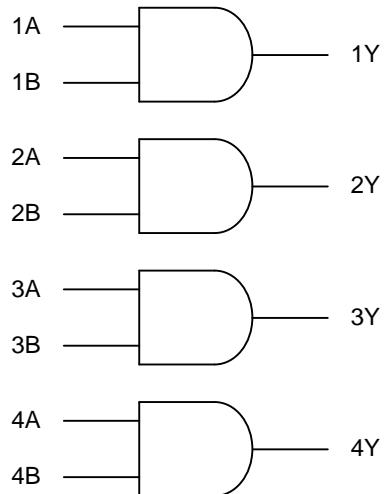
PIN CONFIGURATION

SOP-14		DIP-14	
1A	1	14	VDD
1B	2	13	4B
1Y	3	12	4A
2Y	4	11	4Y
2A	5	10	3Y
2B	6	9	3B
VSS	7	8	3A

PIN DESCRIPTION

Pin No.		Pin Name	Pin Function
SOP-14	DIP-14		
1	1	1A	Input 1A
2	2	1B	Input 1B
3	3	1Y	Output 1
4	4	2Y	Output 2
5	5	2A	Input 2A
6	6	2B	Input 2B
7	7	VSS	Ground
8	8	3A	Input 3A
9	9	3B	Input 3B
10	10	3Y	Output 3
11	11	4Y	Output 4
12	12	4A	Input 4A
13	13	4B	Input 4B
14	14	VDD	Power Supply

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Voltages referenced to V_{SS}.

SYMBOL	PARAMETER	TEST CONDITION	V _{DD}	Limit			UNIT	
				-55°C	25°C	125°C		
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5V or V _{DD} - 0.5V	5 V	3.5	3.5	3.5	V	
		V _{OUT} = 1.0V or V _{DD} - 1.0V	10 V	7	7	7		
		V _{OUT} = 1.5V or V _{DD} - 1.5V	15 V	11	11	11		
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.5V	5 V	1.5	1.5	1.5	V	
		V _{OUT} = 1.0V	10 V	3	3	3		
		V _{OUT} = 1.5V	15 V	4	4	4		
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{DD}	5 V	4.95	4.95	4.95	V	
			10 V	9.95	9.95	9.95		
			15 V	14.95	14.95	14.95		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{DD} or V _{SS}	5 V	0.05	0.05	0.05	V	
			10 V	0.05	0.05	0.05		
			15 V	0.05	0.05	0.05		
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{DD} or V _{SS}	18 V	±0.1	±0.1	±1.0	µA	
I _{CC}	Maximum Quiescent Supply Current		5 V	0.25	0.25	7.5	µA	
	V _{IN} = V _{DD} or V _{SS}	10 V	0.5	0.5	15			
		15 V	1.0	1.0	30			
		20 V	5.0	5.0	150			
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = V _{DD} or V _{SS}	V _{OL} = 0.4V	5 V	0.64	0.51	0.36	mA
			V _{OL} = 0.5V	10 V	1.6	1.3	0.9	
			V _{OL} = 1.5V	15 V	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = V _{DD} or V _{SS}	V _{OH} = 2.5V	5 V	-2.0	-1.6	-1.15	mA
			V _{OH} = 4.6V	5 V	-0.64	-0.51	-0.36	
			V _{OH} = 9.5V	10 V	-1.6	-1.3	-0.9	
			V _{OH} = 13.5V	15 V	-4.2	-3.4	-2.4	

CMOS Quad 2-Input AND Gates

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AC ELECTRICAL CHARACTERISTICS

$C_L = 50 \text{ pF}$, $R_L = 200\text{k}\Omega$, Input $t_r = t_f = 20 \text{ ns}$

SYMBOL	PARAMETER	VDD	Limit			UNIT
			-55°C	25°C	125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or Input B to Output Y (Figure 1)	5 V	250	250	500	ns
		10 V	120	120	240	
		15 V	90	90	180	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5 V	200	200	400	ns
		10 V	100	100	200	
		15 V	80	80	160	
C_{IN}	Maximum Input Capacitance	—		7.5		pF

FUNCTION TABLE

Input (A)	Input (B)	Output (Y)
L	L	L
L	H	L
H	L	L
H	H	H

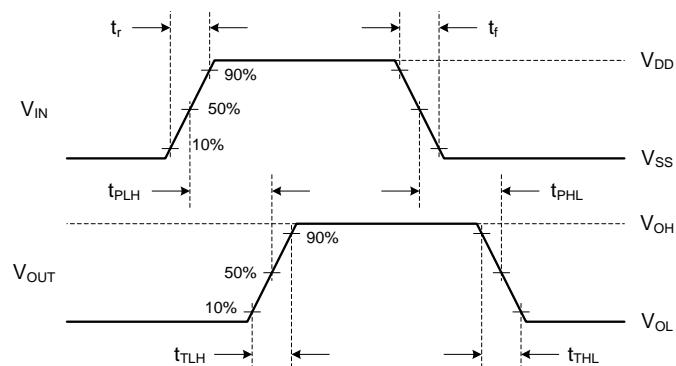
SWITCHING CHARACTERISTICS

Fig. 1. Switching Time Waveforms

TYPICAL OPERATING CHARACTERISTICS

T.B.D.

REVISION NOTICE

The description in this datasheet is subject to change without any notice to describe its electrical characteristics properly.