40V N-Channel MOSFETs

PDC4801R

General Description

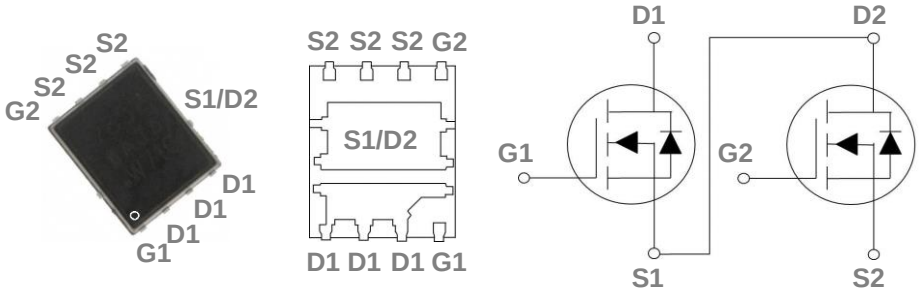
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

	BVDSS	RDSON	ID
Q1	40V	13mΩ	39A
Q2	40V	6.8mΩ	60A

Features

- *Improved dv/dt capability*
- *Fast switching*
- *100% EAS Guaranteed*
- *Green Device Available*

PPAK5x6 Asymmetric Dual Pin Configuration



Applications

- *MB / VGA / Vcore*
- *POL Buck Applications*
- *SMPS 2nd SR*

Absolute Maximum Ratings Tc=25℃ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain-Source Voltage	40	40	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D	Drain Current – Continuous (T_C=25℃)	39	60	A
	Drain Current – Continuous (T_C=100℃)	24.6	37.9	A
I_{DM}	Drain Current – Pulsed[1] , Chip/Package Limit	156	240	A
EAS	Single Pulse Avalanche Energy[2]	58	88	mJ
IAS	Single Pulse Avalanche Current[2]	34	42	A
P_D	Power Dissipation (T_C=25℃)	34.7	41.7	W
	Power Dissipation – Derate above 25℃	0.28	0.33	W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Characteristics

Symbol		Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Q1	Thermal Resistance Junction to ambient	---	62	℃/W
$R_{\theta JA}$	Q2		---	62	℃/W
$R_{\theta JC}$	Q1	Thermal Resistance Junction to Case	'---	3.6	℃/W
$R_{\theta JC}$	Q2		'---	3	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Static State Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	Q1	40	---	---	V
			Q2	40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=1mA	Q1	---	---	---	V/℃
			Q2	---	0.03	---	V/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=40V , V_{GS}=0V , T_J=25℃	Q1	---	---	1	uA
			Q2	---	---	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=125℃	Q1	---	---	10	uA
			Q2	---	---	10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	Q1	---	---	±100	nA
			Q2	---	---	±100	nA
$R_{DS(ON)}$	Static Drain-Source On-Resistance[3]	V_{GS}=10V , I_D=8A	Q1	---	9	13	mΩ
		V_{GS}=10V , I_D=10A	Q2	---	5.5	6.8	mΩ
		V_{GS}=4.5V , I_D=6A	Q1	---	11.5	17	mΩ
		V_{GS}=4.5V , I_D=5A	Q2	---	7.2	9.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	Q1	1	1.6	2.5	V
			Q2	1	1.6	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		Q1	---	---	---	mV/℃
			Q2	---	-5	---	mV/℃
gfs	Forward Transconductance	V_{DS}=10V , I_D=1A	Q1	---	5	---	S
		V_{DS}=10V , I_D=3A	Q2	---	10	---	S

Dynamic Characteristics

Q_g	Total Gate Charge[3,4]	V_{DS}=20V , V_{GS}=4.5V , I_D=10A	Q1	---	13	26	nC
			Q2	---	16.2	32	
Q_{gs}	Gate-Source Charge[3,4]		Q1	---	4	8	
			Q2	---	3.85	7	
Q_{gd}	Gate-Drain Charge[3,4]		Q1	---	5.3	10	
			Q2	---	6.05	12	
$T_{d(on)}$	Turn-On Delay Time[3,4]	V_{DD}=20V , V_{GS}=10V , R_G=6Ω I_D=1A	Q1	---	8	16	ns
			Q2	---	13.6	25	
T_r	Rise Time[3,4]		Q1	---	3.2	8	
			Q2	---	2.5	5	
$T_{d(off)}$	Turn-Off Delay Time[3,4]		Q1	---	26.4	52	
			Q2	---	68	120	
T_f	Fall Time[3,4]		Q1	---	3.8	8	
			Q2	---	5	10	

C_{iss}	Input Capacitance	V_{DS}=25V , V_{GS}=0V , F=1MHz	Q1	---	1088	2000	pF
			Q2	---	1540	2500	
C_{oss}	Output Capacitance		Q1	---	110	200	
			Q2	---	171	330	
C_{rss}	Reverse Transfer Capacitance		Q1	---	80	160	
			Q2	---	115	220	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz	Q1	---	3	---	Ω
			Q2	---	1.2	---	Ω

Drain-Source Diode Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	Q1	---	---	39	A
			Q2	---	---	60	A
I_{SM}	Pulsed Source Current[3]		Q1	---	---	78	A
			Q2	---	---	120	A
V_{SD}	Diode Forward Voltage[3]	V_{GS}=0V , I_S=1A , T_J=25℃	Q1	---	---	1	V
			Q2	---	---	1	V

Note :
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V,V_{GS}=10V,L=0.1mH,Q1:I_{AS}=34A,Q2:I_{AS}=42A,R_G=25Ω,Starting T_J=25℃.
3. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

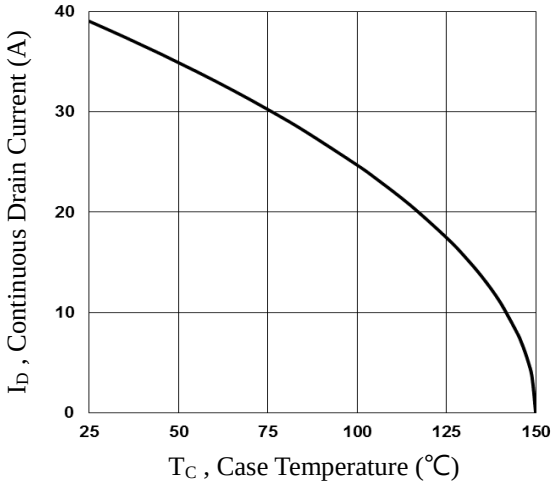


Fig.1 Q1 Continuous Drain Current vs. T_C

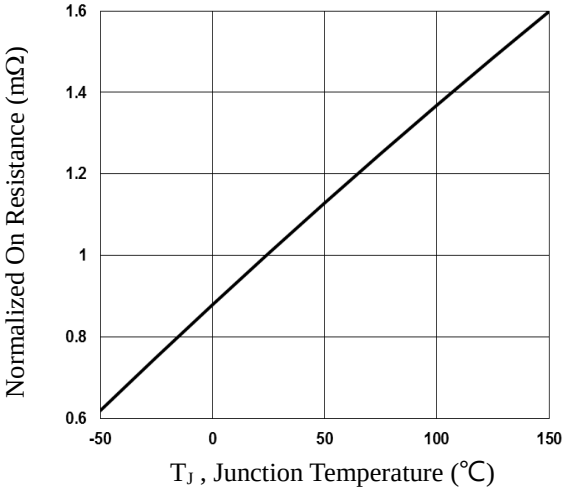


Fig.2 Q1 Normalized RDSON vs. T_J

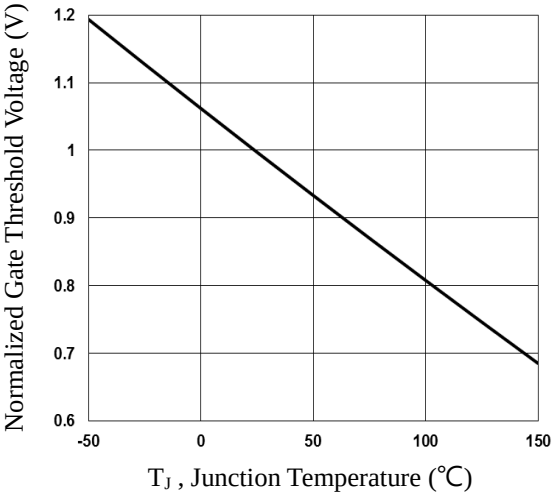


Fig.3 Q1 Normalized V_{th} vs. T_J

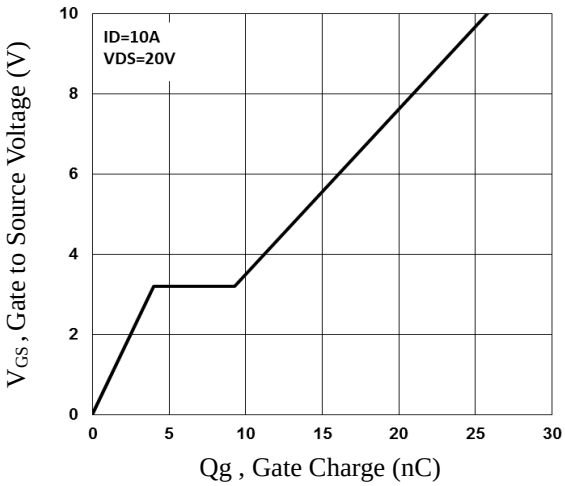


Fig.4 Q1 Gate Charge Waveform

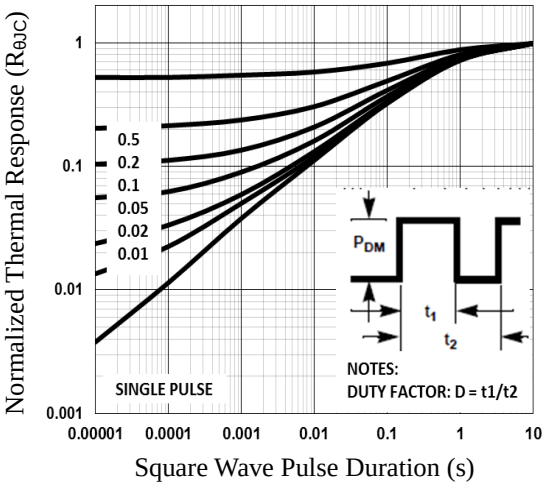


Fig.5 Q1 Normalized Transient Impedance

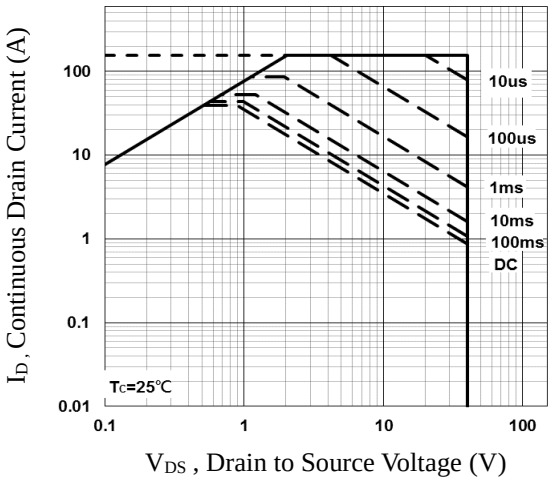


Fig.6 Q1 Maximum Safe Operation Area

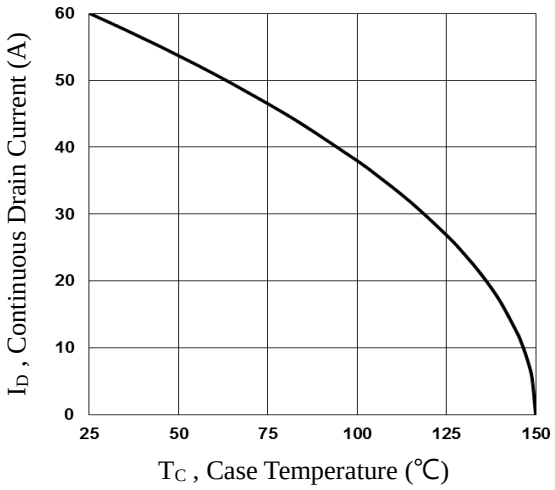


Fig.7 Q2 Continuous Drain Current vs. T_C

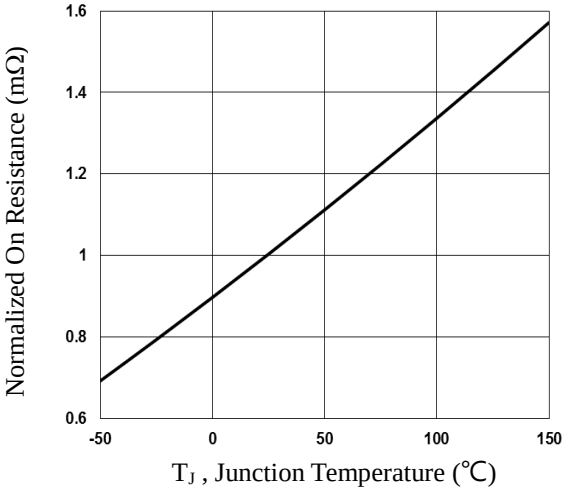


Fig.8 Q2 Normalized RDSON vs. T_J

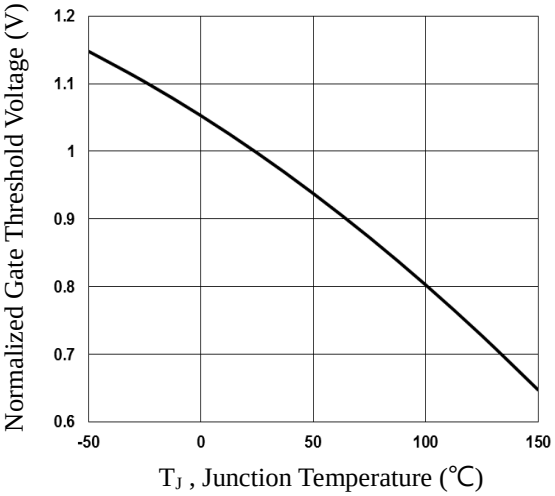


Fig.9 Q2 Normalized V_{th} vs. T_J

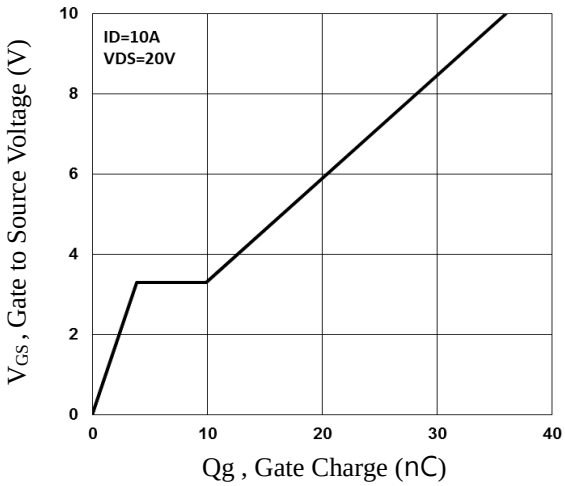


Fig.10 Q2 Gate Charge Waveform

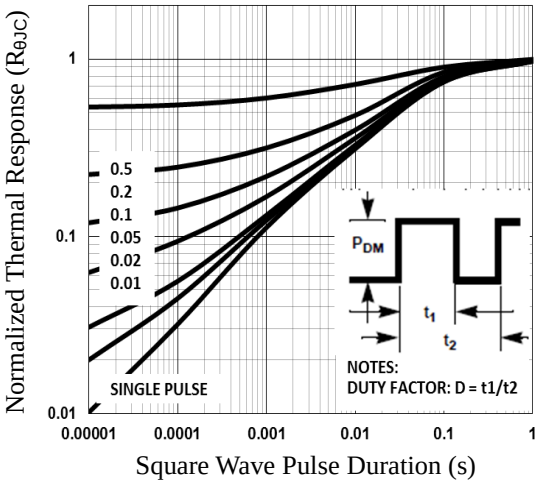


Fig.11 Q2 Normalized Transient Impedance

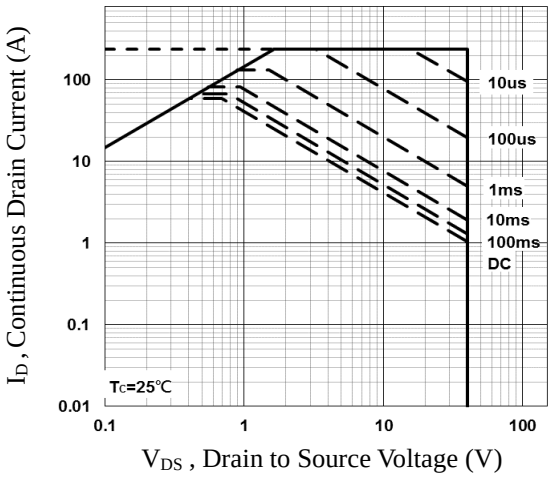


Fig.12 Q2 Maximum Safe Operation Area

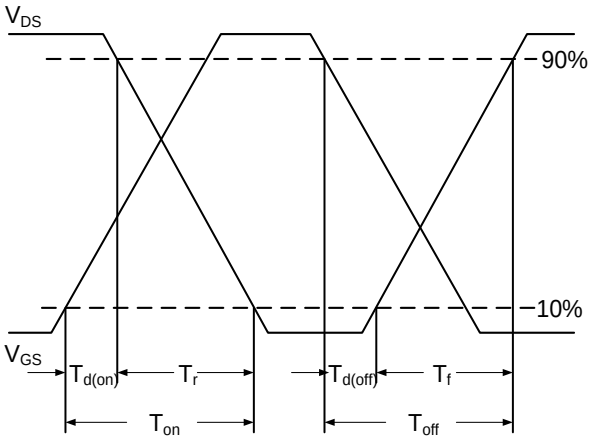


Fig.13 Switching Time Waveform

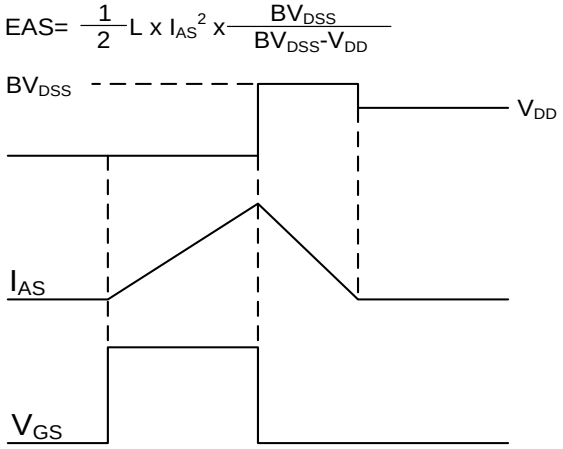
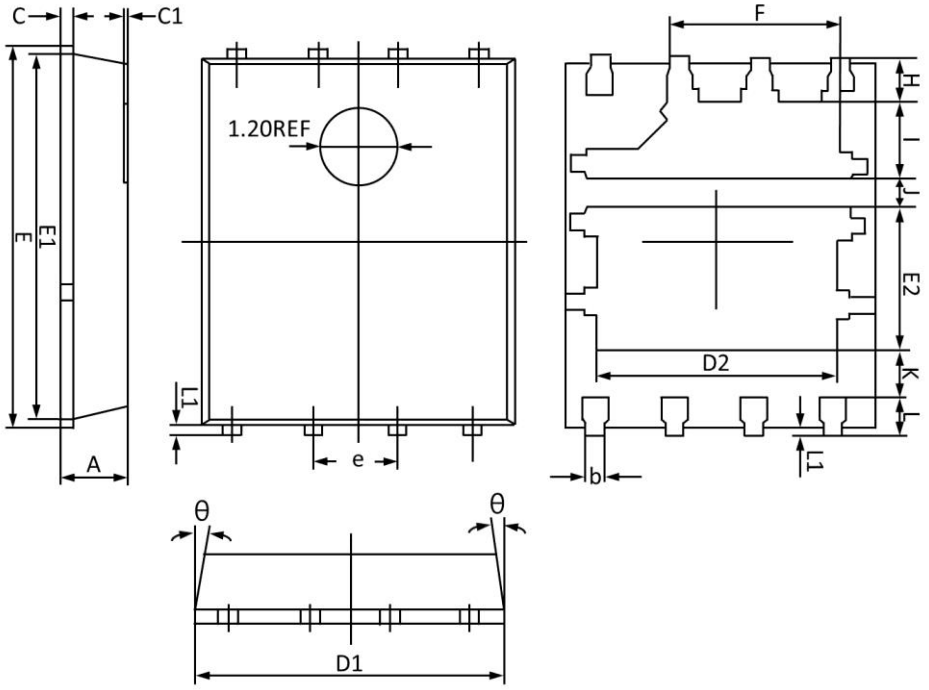


Fig.14 EAS Waveform

PPAK5x6 Asymmetric Dual Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.036	0.043
b	0.330	0.510	0.013	0.020
C	0.200	0.300	0.008	0.011
C1	0.040 REF		0.040 REF	
D1	4.800	5.000	0.189	0.196
D2	3.610	3.960	0.143	0.155
E	5.900	6.100	0.233	0.240
E1	5.700	5.800	0.225	0.228
E2	2.020	2.420	0.080	0.095
e	1.270BSC		1.270BSC	
F	2.550	2.900	0.101	0.114
H	0.610	0.810	0.025	0.031
I	1.100	1.300	0.044	0.051
J	0.400	0.600	0.016	0.023
K	0.500	-	0.020	-
L	0.510	0.710	0.020	0.027
L1	0.060	0.200	0.003	0.007
θ	0°	12°	0°	12°