1. General description

The XL9555 is a 24-pin CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I^2C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I^2C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The XL9555 consists of two 8-bit Configurati on (Input or Output selection); Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I^2C-bus address compatible with the 8575, software changes are required due to the enhancements, and are discussed in *Application Note AN469*.

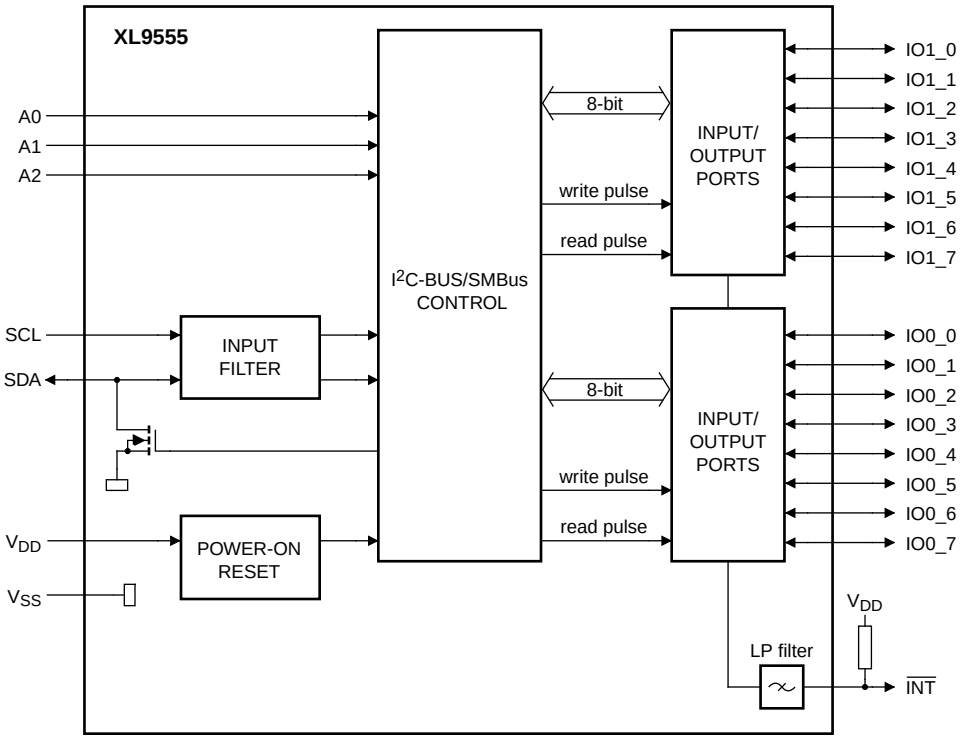
The XL9555 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I^2C-bus address and allow up to eight devices to share the same I^2C-bus/SMBus. The fixed I^2C-bus address of the XL9555 is the same as the XL9554, allowing up to eight of these devices in any combination to share the same I^2C-bus/SMBus.

2. Features and benefits

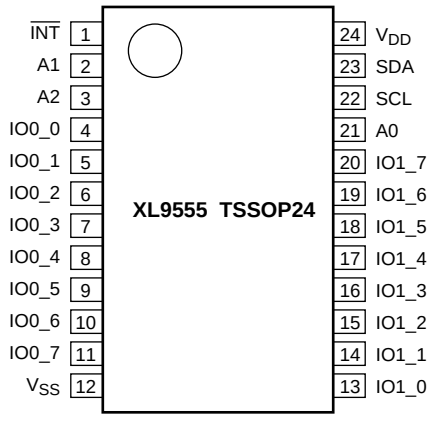
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101

3. Block diagram



Remark: All I/Os are set to inputs at reset.

Block diagram of XL9555



Pin configuration for TSSOP24

4. Pin description

Pin description

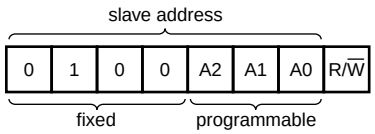
Symbol	Pin	Description
	TSSOP24	
$\overline{INT}$	1	interrupt output (open-drain)
A1	2	address input 1
A2	3	address input 2
IO0_0	4	port 0 input/output
IO0_1	5	
IO0_2	6	
IO0_3	7	
IO0_4	8	
IO0_5	9	
IO0_6	10	
IO0_7	11	
V_{SS}	12	supply ground
IO1_0	13	port 1 input/output
IO1_1	14	
IO1_2	15	
IO1_3	16	
IO1_4	17	
IO1_5	18	
IO1_6	19	
IO1_7	20	
A0	21	address input 0
SCL	22	serial clock line
SDA	23	serial data line
V_{DD}	24	supply voltage

[1] HVQFN and HWQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

5. Functional description

Refer to Figure 1 “Block diagram of XL9555”.

5.1 Device address



XL9555 device address

5.2 Registers

5.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

5.2.2 Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Input port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

5.2.3 Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

5.2.4 Registers 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Polarity Inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

5.2.5 Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to V_{DD} at each pin. At reset, the device's ports are inputs with a pull-up to V_{DD}.

Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

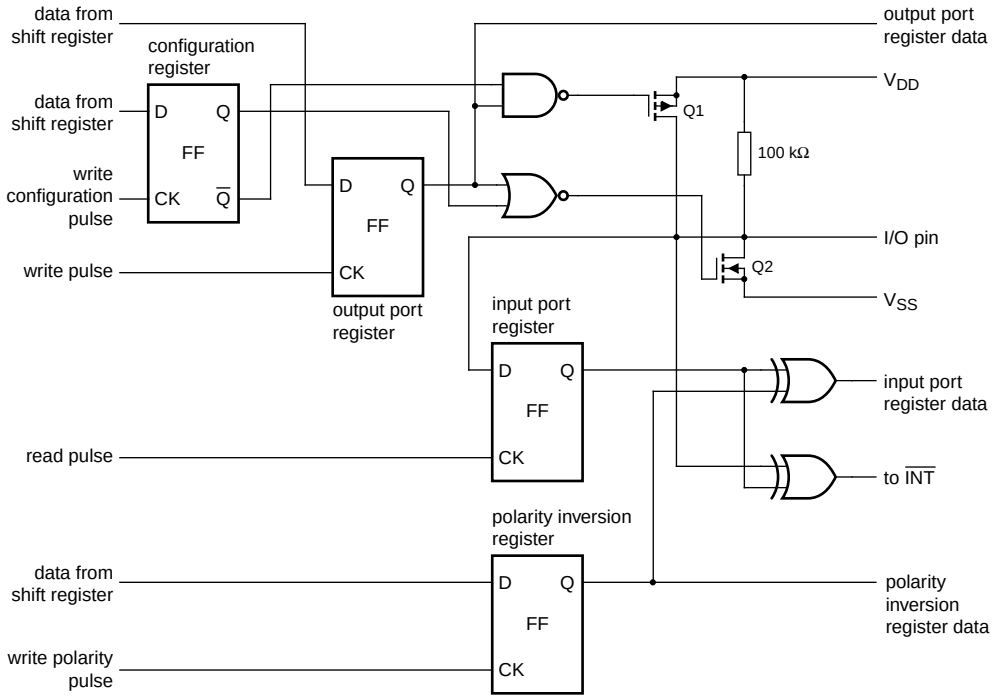
5.3 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the XL9555 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the XL9555 registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

5.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.



At power-on reset, all registers return to default values.

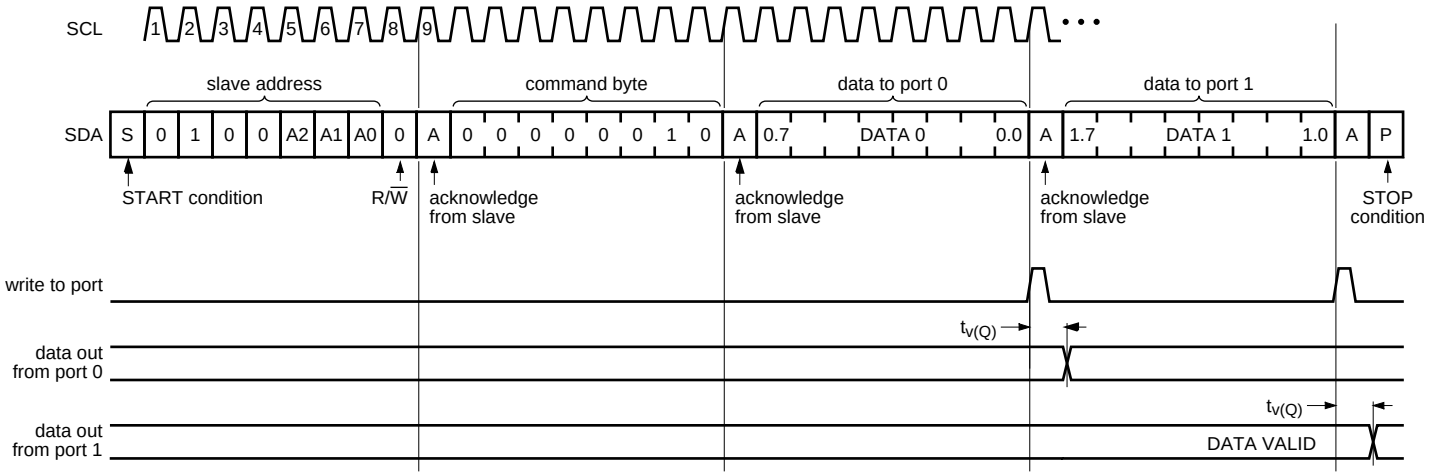
Simplified schematic of I/Os

5.5 Bus transactions

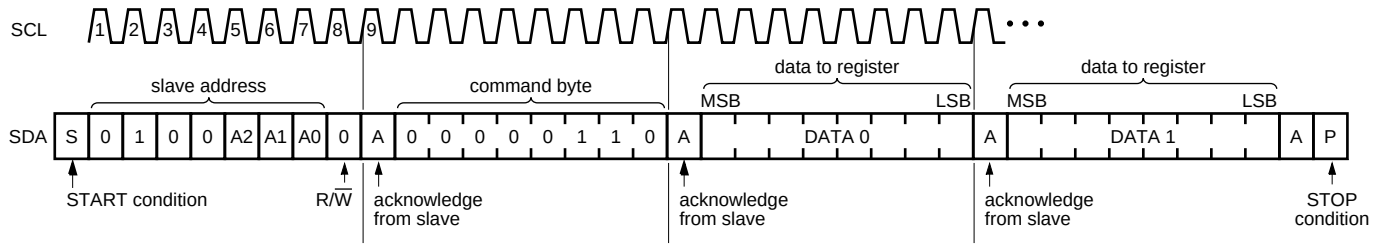
5.5.1 Writing to the port registers

Data is transmitted to the XL9555 by sending the device address and setting the least significant bit to a logic 0 (see Figure 8 “XL9555 device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the XL9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 10 and Figure 11). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.



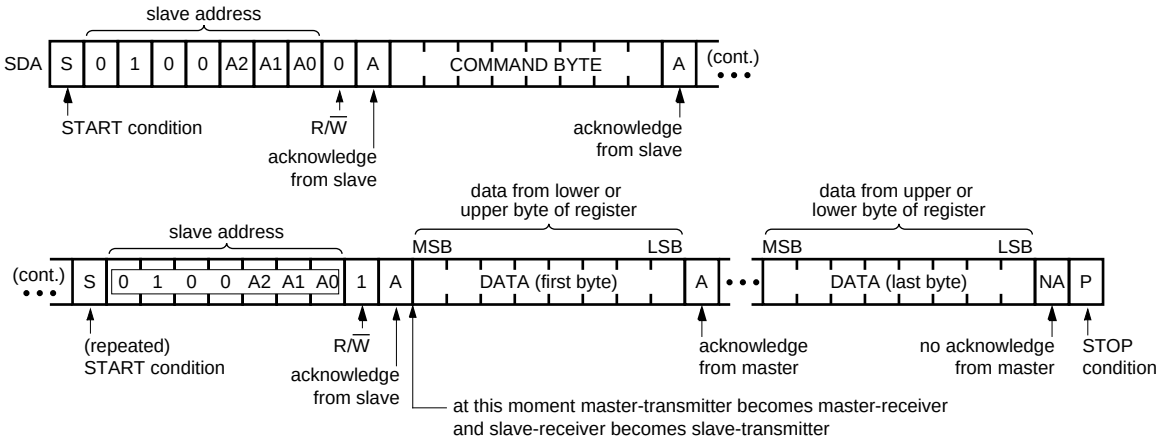
Write to Output port registers



Write to Configuration registers

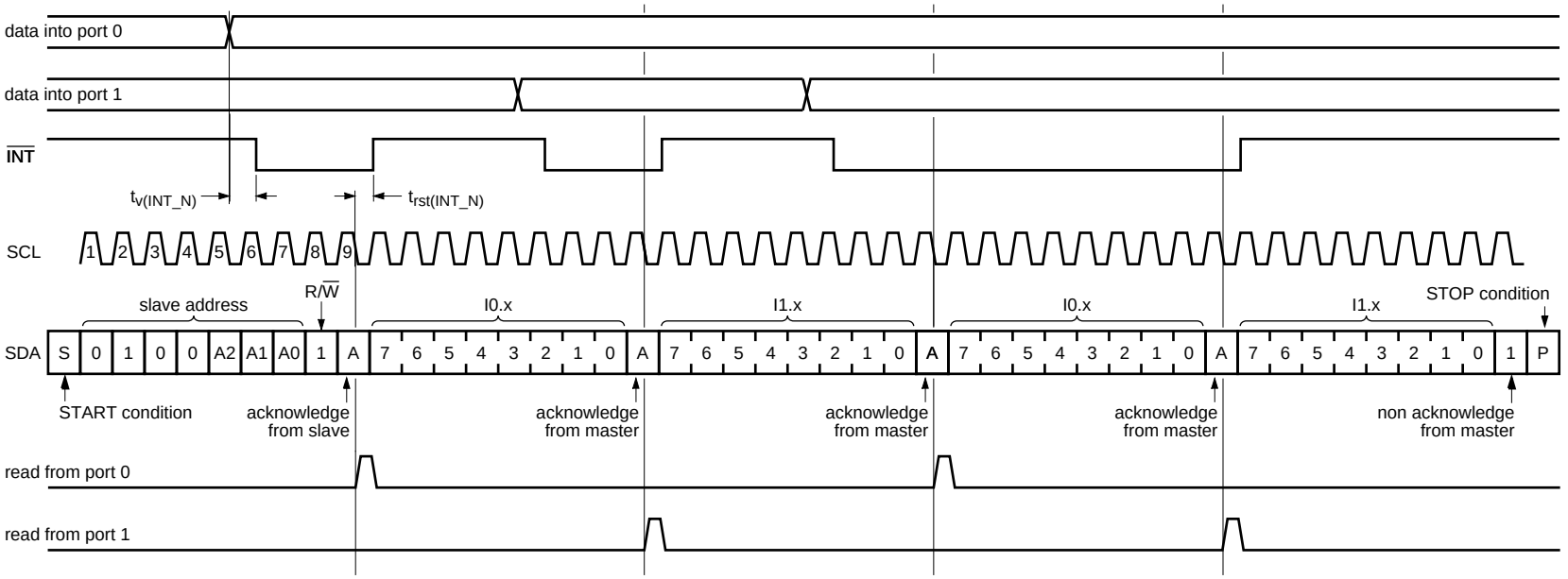
5.5.2 Reading the port registers

In order to read data from the XL9555, the bus master must first send the XL9555 address with the least significant bit set to a logic 0 (see Figure 8 “XL9555 device address”). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the XL9555 (see Figure 12, Figure 13 and Figure 14). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.



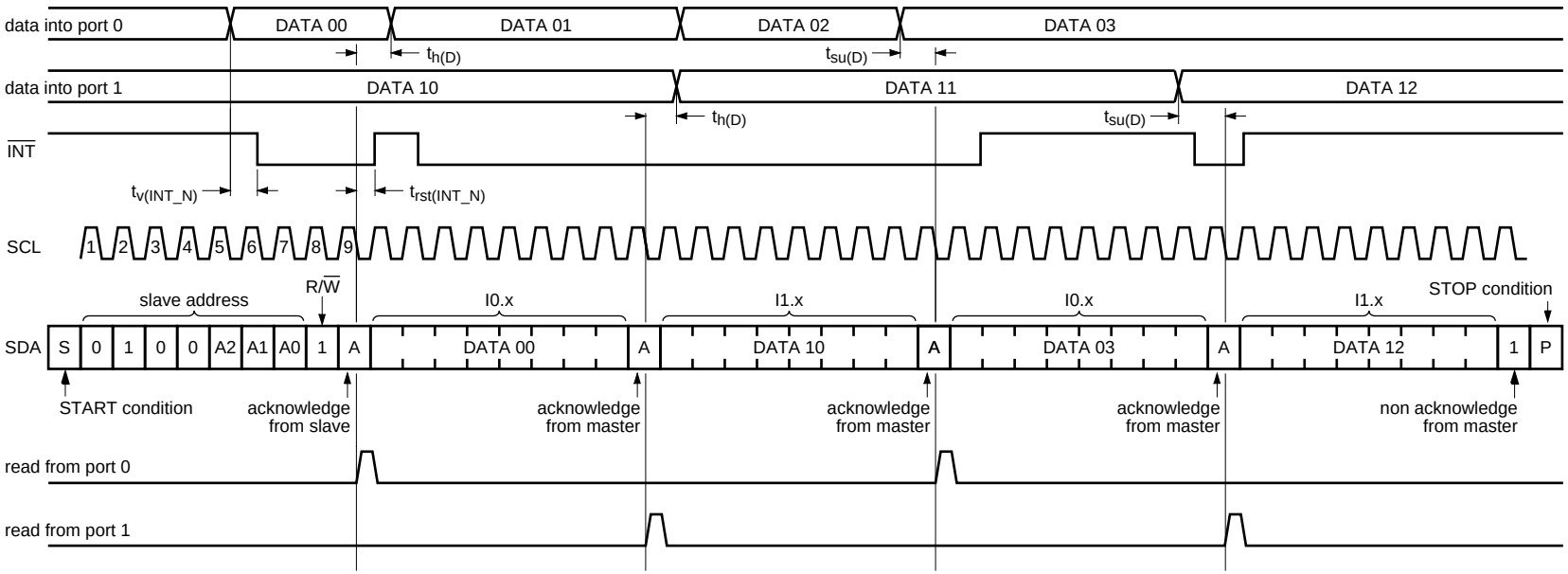
Remark: Transfer can be stopped at any time by a STOP condition.

Read from register



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Read Input port register, scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Read Input port register, scenario 2

6. Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 13). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

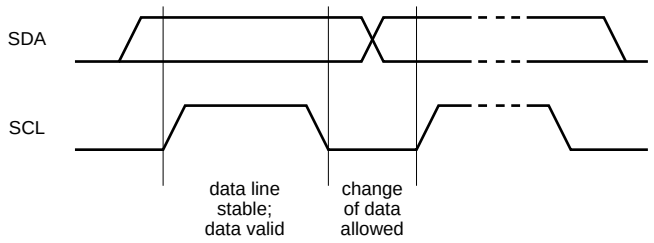
Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

7. Characteristics of the I^2C-bus

The I^2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

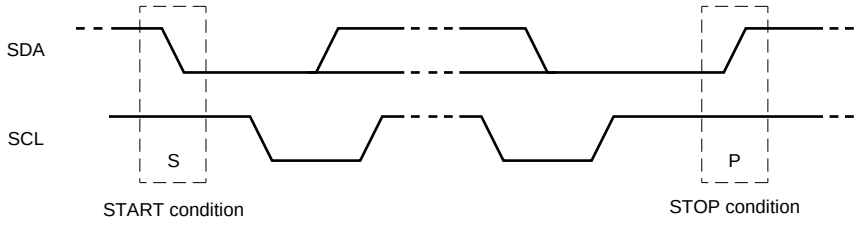
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).



Bit transfer

7.1.1 START and STOP conditions

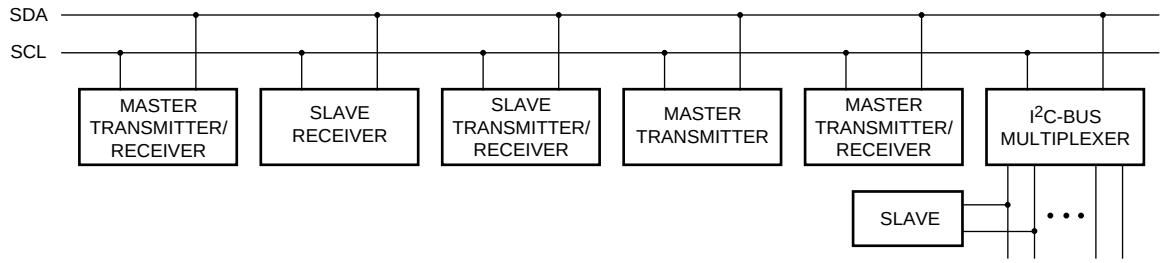
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16).



Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 17).



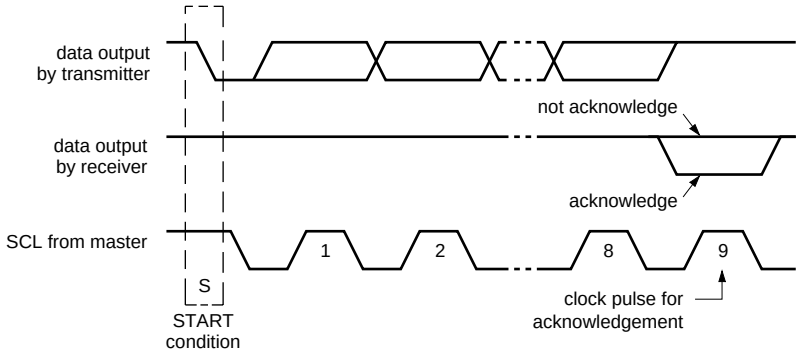
System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

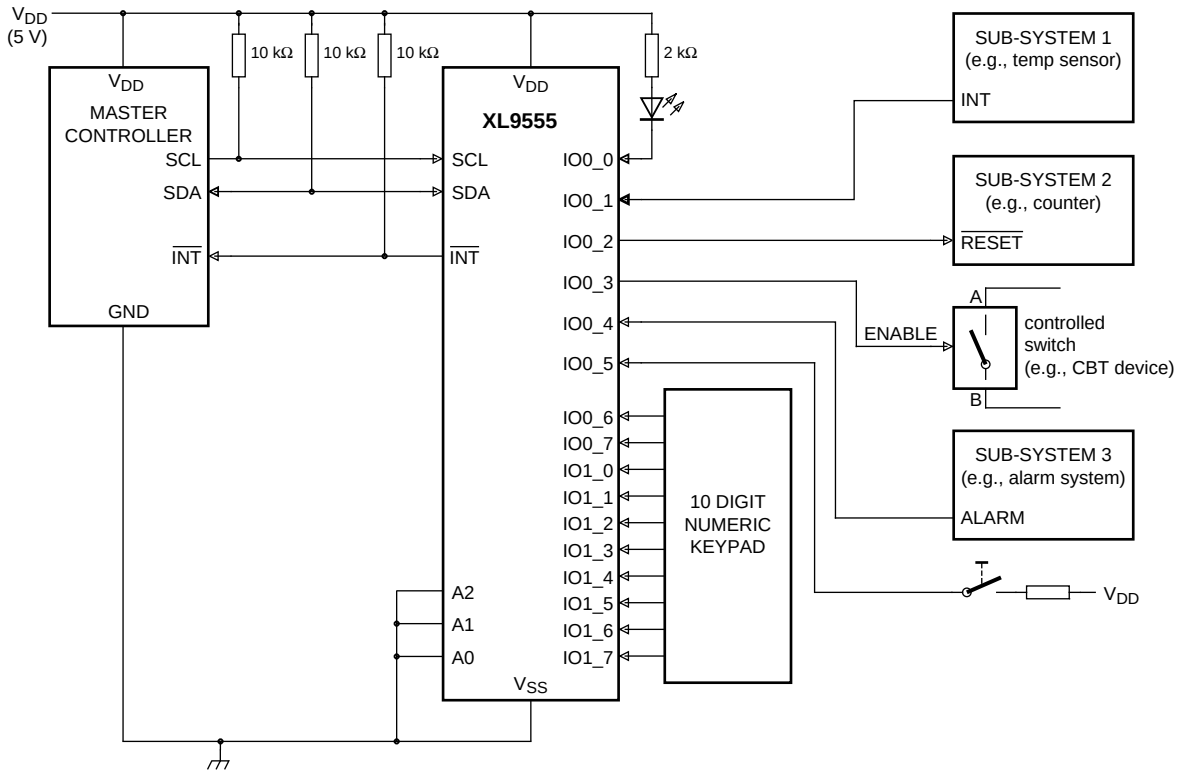
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



Acknowledgement on the I 2C-bus

8. Application design-in information



Device address configured as 0100 000xb for this example.

IO0_0, IO0_2, IO0_3 configured as outputs.

IO0_1, IO0_4, IO0_5 configured as inputs.

IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Typical application

9. Limiting values

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} − 0.5	6	V
I_O	output current	on an I/O pin		-	±50	mA
I_I	input current			-	±20	mA
I_{DD}	supply current			-	160	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature	operating		−40	+85	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

10. Static characteristics

Static characteristics

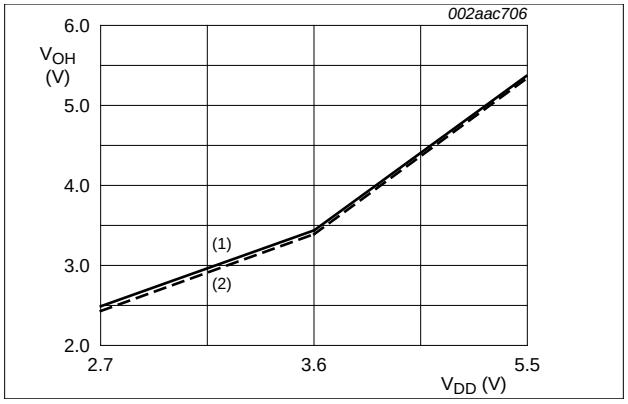
V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz		-	135	200	μA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs		-	1.1	1.5	mA
		Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	μA
V_{POR}	power-on reset voltage[1]	no load; V_I = V_{DD} or V_{SS}		-	1.5	1.65	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}		−1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.5 V	[2]	8	(8 to 20)	-	mA
		V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.7 V	[2]	10	(10 to 24)	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V	[3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 5.5 V; V_I = V_{DD}		-	-	1	μA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}		-	-	−100	μA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF
Interrupt $\overline{INT}$							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
Select inputs A0, A1, A2							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V for at least 5 μs in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_1 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

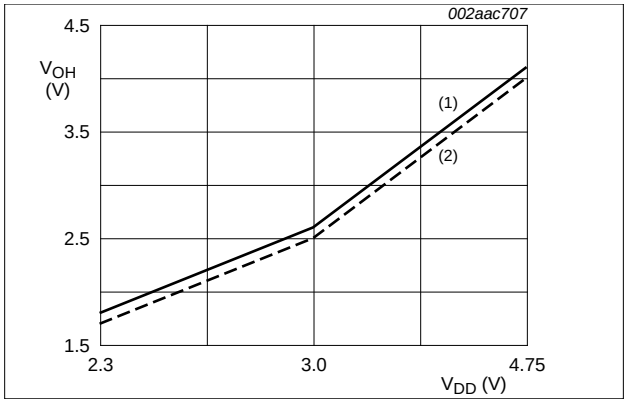
[3] The total current sourced by all I/Os must be limited to 160 mA.



(1) I_{OH} = –8 mA

(2) I_{OH} = –10 mA

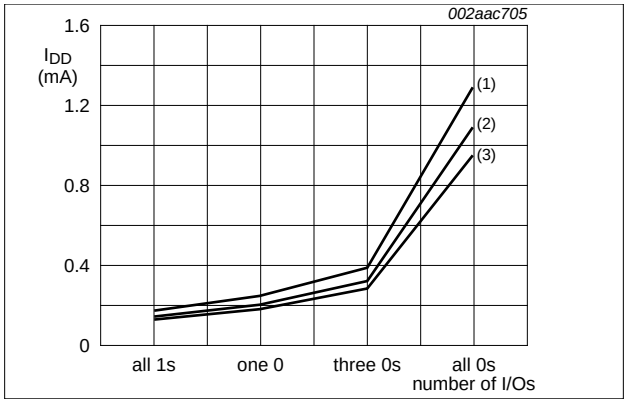
V_{OH} maximum



(1) I_{OH} = –8 mA

(2) I_{OH} = –10 mA

V_{OH} minimum



V_{DD} = 5.5 V; $V_{I/O}$ = 5.5 V; A2, A1, A0 set to logic 0.

(1) T_{amb} = –40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

I_{DD} versus number of I/Os held LOW

11. Dynamic characteristics

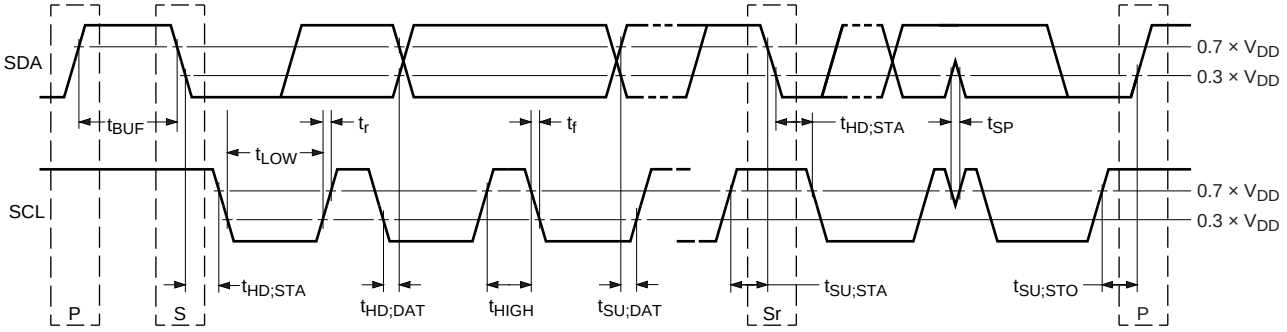
Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{VD;ACK}$	data valid acknowledge time		[1]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;DAT}$	data valid time		[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$ [3]	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time			-	200	-	200	ns
$t_{su(D)}$	data input set-up time			150	-	150	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs
Interrupt timing								
$t_{v(INT\_N)}$	valid time on pin $\overline{INT}$			-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$			-	4	-	4	µs

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

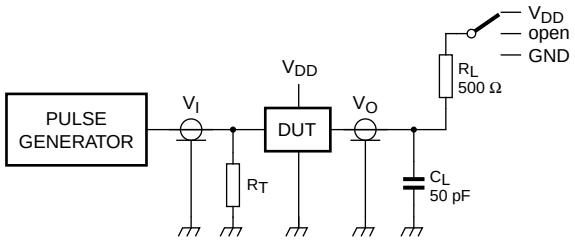
[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.



Definition of timing on the I²C-bus

12. Test information

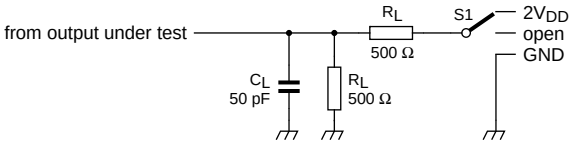


R_L = load resistor.

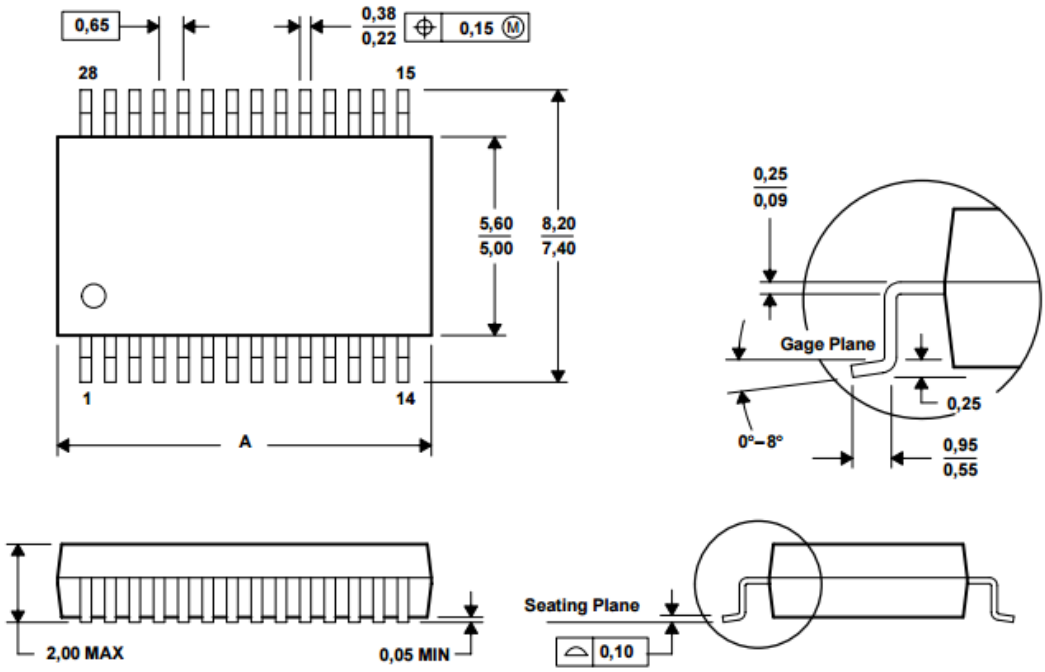
C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Test circuitry for switching times



Load circuit



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA