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XD74HC597 DIP16
XL74HC597 SOP16

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	SH_{CP} to Q		17	20	ns
	ST_{CP} to Q		25	29	ns
	$\overline{PL}$ to Q		21	26	ns
f_{max}	maximum clock frequency SH_{CP}		96	83	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	29	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH_{CP}	shift clock input (LOW-to-HIGH, edge-triggered)
12	ST_{CP}	storage clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	parallel load input (active LOW)
14	D_S	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D_0 to D_7	parallel data inputs
16	V_{CC}	positive supply voltage

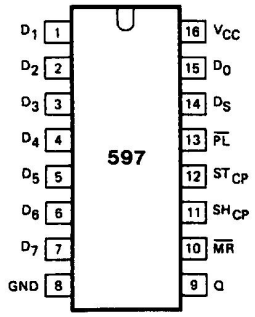


Fig.1 Pin configuration.

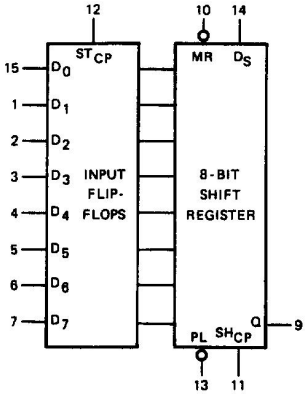


Fig.2 Logic symbol.

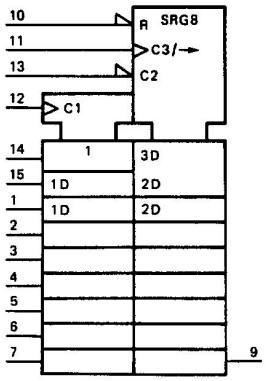


Fig.3 IEC logic symbol.

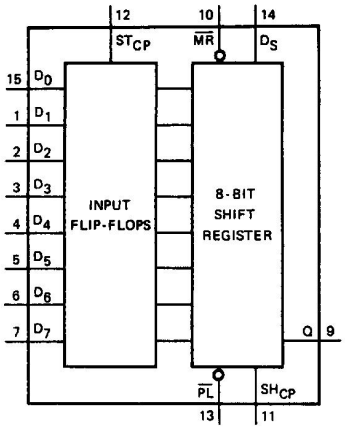


Fig.4 Functional diagram.

FUNCTION TABLE

ST_{CP}	SH_{CP}	$\overline{PL}$	$\overline{MR}$	FUNCTION
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = D_S$

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH CP transition

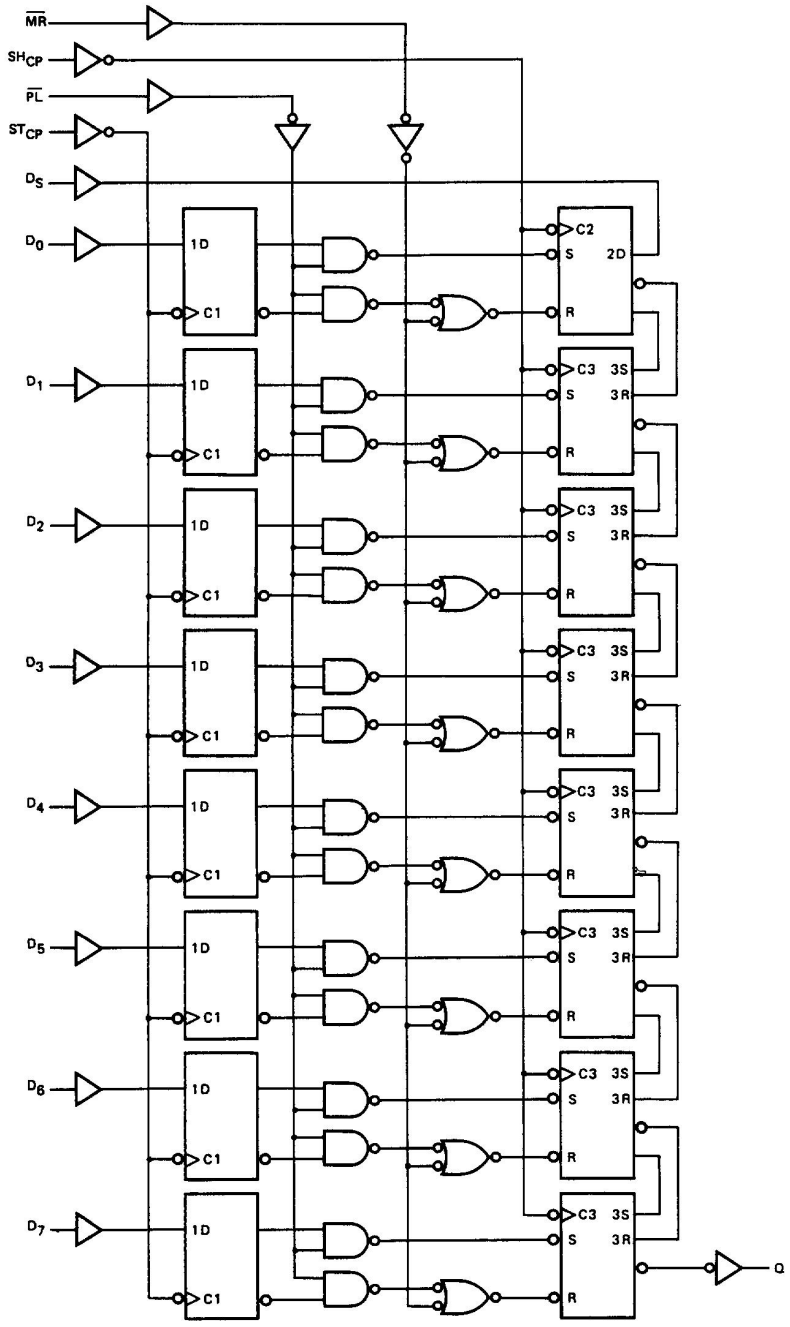


Fig.5 Logic diagram.

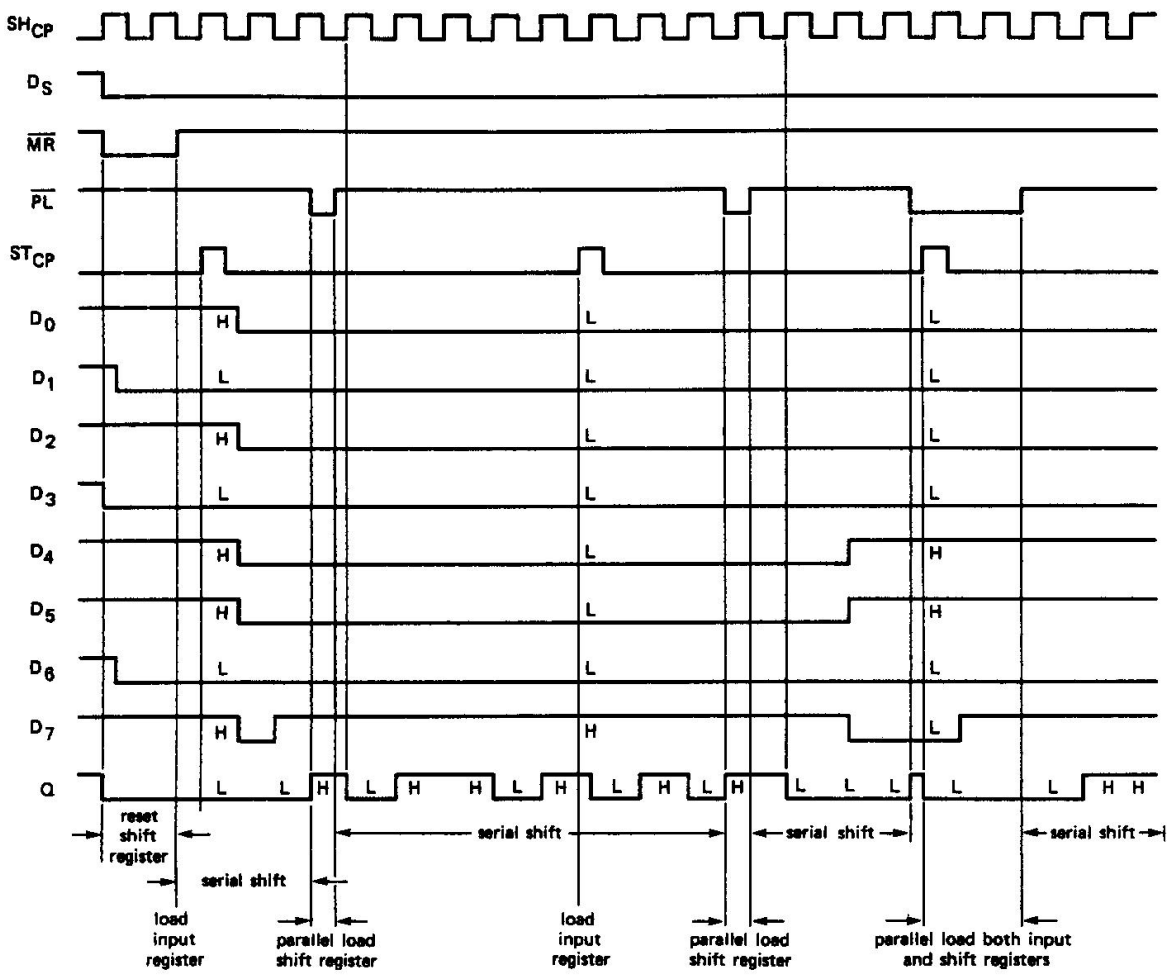


Fig.6 Timing diagram.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC597								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay SH_{CP} to Q		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t_{PHL}	propagation delay $\overline{MR}$ to Q		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay ST_{CP} to Q		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to Q		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t_W	ST_{CP} pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_W	SH_{CP} pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_W	$\overline{MR}$ pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_W	$\overline{PL}$ pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	60 12 10	–3 –1 –1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.10
t_{su}	set-up time D_n to ST_{CP}	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC597								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time D_S to SH_{CP}	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.12
t_h	hold time D_n to ST_{CP}	5 5 5	−3 −1 −1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.11
t_h	hold time $\overline{PL}$, D_S to SH_{CP}	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.11
f_{max}	maximum pulse frequency SH_{CP}	6.0 30 35	29 87 104		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

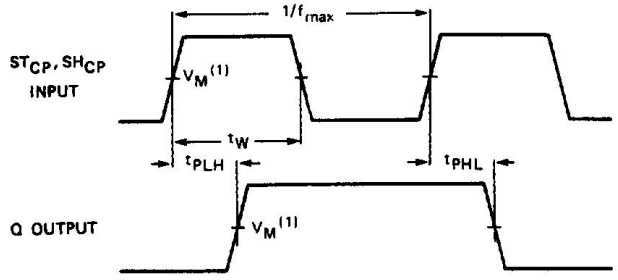
INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
D_n	0.30
$\overline{PL}$, $\overline{MR}$	1.50
ST_{CP}, SH_{CP}	1.50

AC WAVEFORMS FOR 74HC597

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

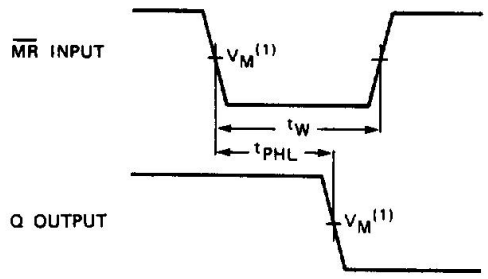
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC597								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay SH_{CP} to Q		23	40		50		60	ns	4.5	Fig.7
t_{PHL}	propagation delay $\overline{MR}$ to Q		28	49		61		74	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay ST_{CP} to Q		33	57		71		86	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to Q		30	52		65		78	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.9
t_W	SH_{CP} pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.7
t_W	ST_{CP} pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig.7
t_W	$\overline{MR}$ pulse width LOW	25	14		31		38		ns	4.5	Fig.8
t_W	$\overline{PL}$ pulse width LOW	20	10		25		30		ns	4.5	Fig.9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	12	–2		15		18		ns	4.5	Fig.10
t_{su}	set-up time D_n to ST_{CP}	12	5		15		18		ns	4.5	Fig.11
t_{su}	set-up time D_S to SH_{CP}	12	2		15		18		ns	4.5	Fig.11
t_{su}	set-up time $\overline{PL}$ to SH_{CP}	12	4		15		18		ns	4.5	Fig.12
t_h	hold time D_n to ST_{CP}	5	–1		5		5		ns	4.5	Fig.11
t_h	hold time $\overline{PL}$, D_S to SH_{CP}	5	–2		5		5		ns	4.5	Fig.11
f_{max}	maximum pulse frequency SH_{CP}	30	75		24		20		MHz	4.5	Fig.7

AC WAVEFORMS



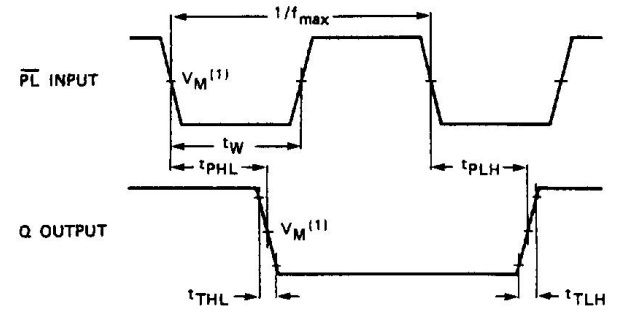
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the SH_{CP} and ST_{CP} inputs to Q output propagation delays, the SH_{CP} and ST_{CP} pulse widths and maximum clock pulse frequency.



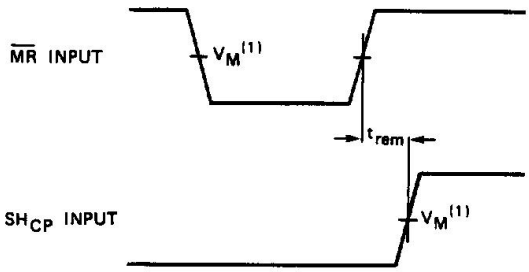
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the $\overline{MR}$ input to Q output propagation delays and the $\overline{MR}$ pulse width.



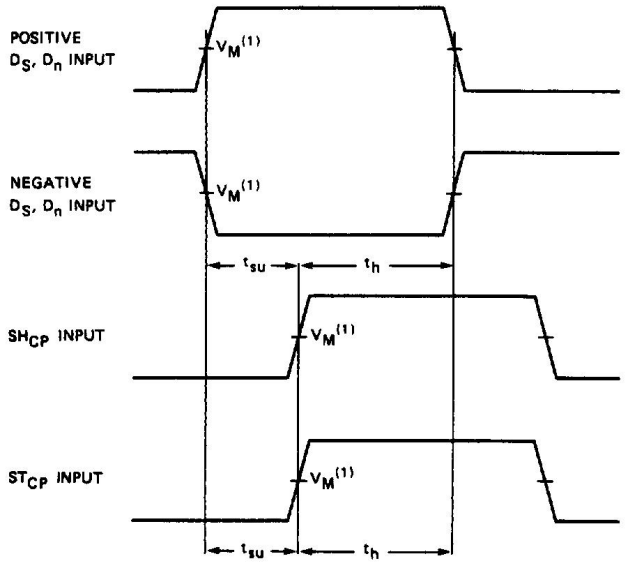
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the $\overline{PL}$ input to Q output propagation delays, $\overline{PL}$ pulse width and output transition times.



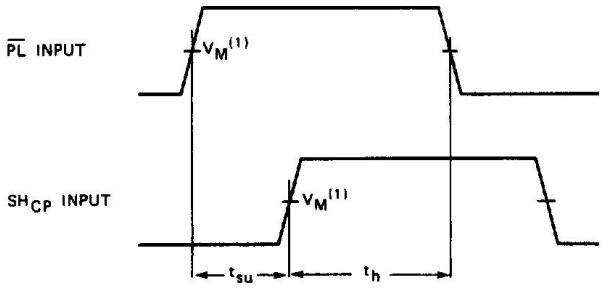
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing the $\overline{MR}$ input to SH_{CP}, ST_{CP} removal times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing hold and set-up times for D_S, D_n inputs to SH_{CP}, ST_{CP} inputs.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.12 Waveforms showing set-up times for $\overline{PL}$ input to SH_{CP} input.