CMT8100, CMT8101 High Reliability Bidirectional I2C Isolators

Features

- Up to 5000 Vrms insulation voltage
- I2C Clock rate: up to 2 MHz
- Power supply voltage: 2.5 V to 5.5 V
- AEC-Q100 Grade 1 qualified
- High CMTI: 150 kV/us
- Chip level ESD: HBM: ±6 kV
- High system level EMC performance:
  - Enhanced system level ESD, EFT, surge immunity
- Isolation barrier life: > 60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15 ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOIC-8 narrow body
  - SOIC-16 wide body
- Safety regulatory approvals
  - UL recognition: up to 5000 Vrms for 1 minute per UL1577
  - CQC certification per GB4943.1-2011
  - CSA component notice 5A
  - DIN VDE V 0884-11:2017-01

Applications

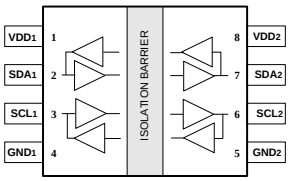
- Power over Ethernet
- Isolated I2C, SMBus, or PMBus interface
- I2C level shifting
- Battery management

Description

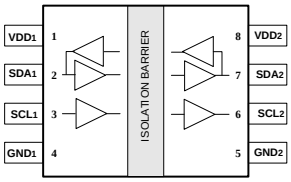
The (CMT8100,CMT8101) devices are high reliability bidirectional isolators that are compatible with I2C interface. The CMT810x devices are AEC-Q100 qualified. The CMT810x devices are safety certified by UL1577 supporting several insulation withstand voltages (3.75 kVrms, 5 kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I2C clock of the CMT810x is up to 2 MHz, and the common-mode transient immunity (CMTI) is up to 150 kV/us. Wide supply voltage of the CMT810x devices supports to connect with most digital interfaces directly, easy to do the level shift. High system level EMC performance enhances device reliability and stability.

Device Information

Part No.	Package	Body Size (mm x mm)
CMT810x	NB(N) SOIC-8	4.9 x 3.9
	WB(W) SOIC-16	10.4 x 7.5
Refer to section 9 for ordering information.		



CMT8100N SOIC8



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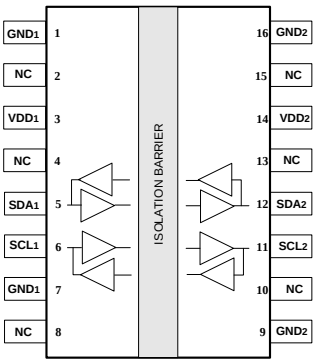
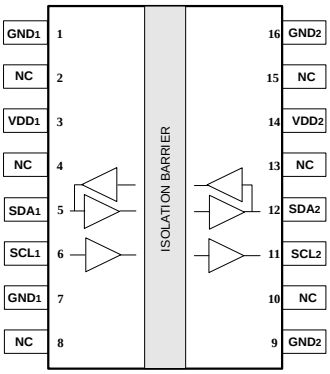


CMT8100W SOIC16 Wide Body



CMT8101W SOIC16 Wide Body

Table of Contents

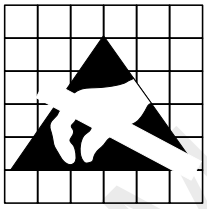
1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameters	Symbol	Condition	Min.	Typ	Max	Unit
Power supply voltage	VDD1, VDD2		-0.5		6.5	V
Maximum input voltage	SDA1, SDA2, SCL1, SCL2		-0.4		VDD+0.4[1]	V
Maximum input pulse voltage	SDA1, SDA2, SCL1, SCL2	Pulse width should be less than 100 ns, and the duty cycle should be less than 10%	-0.8		VDD+0.8	V
Common-Mode transients	CMTI				±150	kV/us
Output current	Io		-15		15	mA
Maximum surge isolation voltage	VIOSM				5.3	kV
Operating temperature	Topr		-40		125	℃
Storage temperature	Tstg		-40		150	℃
Electrostatic discharge	HBM				±6000	V
	CDM				±2000	V

Notes:

[1]. The maximum voltage must not exceed 6.5 V.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

2 Pin Description

Both narrow-body (N) 8-pin and wide-body (W) 16-pin SOIC packages are available for the series part number CMT8100x, CMT8101x. The pin lists are shown as follows.

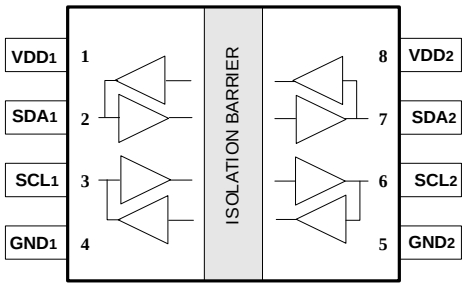


Figure 1. CMT8100N Pin List

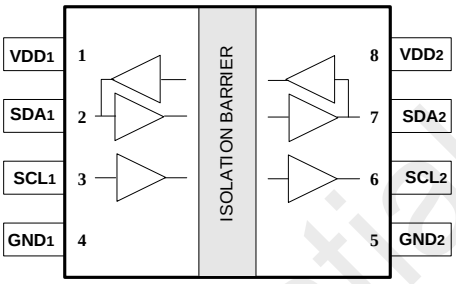


Figure 2. CMT8101N Pin List

Table 2. CMT8100N/8101N Pin Description

Pin #	Pin Name	I/O	Description
1	VDD_1	-	Power supply for isolator side 1.
2	SDA_1	I/O	Serial data input /output, side 1
3	SCL_1	I/O	Serial clock input /output, side 1.
4	GND_1	-	The ground reference for isolator side 1.
5	GND_2	-	The ground reference for isolator side 2.
6	SCL_2	I/O	Serial clock input /output, side 2.
7	SDA_2	I/O	Serial data input /output, side 2
8	VDD_2	-	Power supply for isolator side 2.

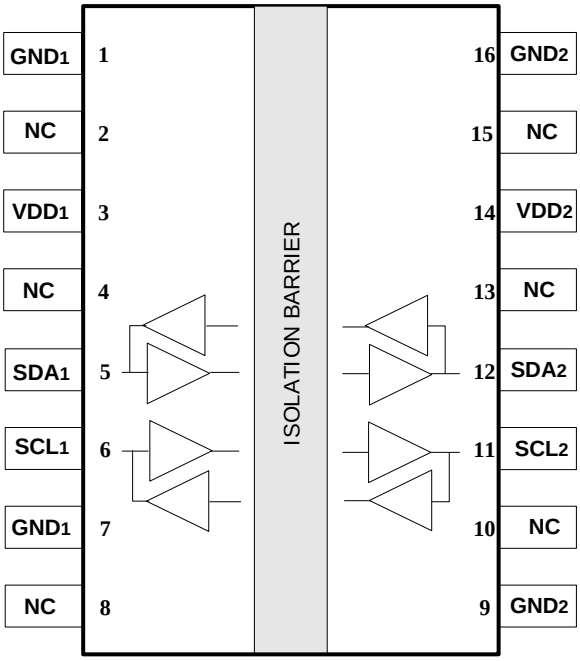


Figure 3 CMT8100W Pin List

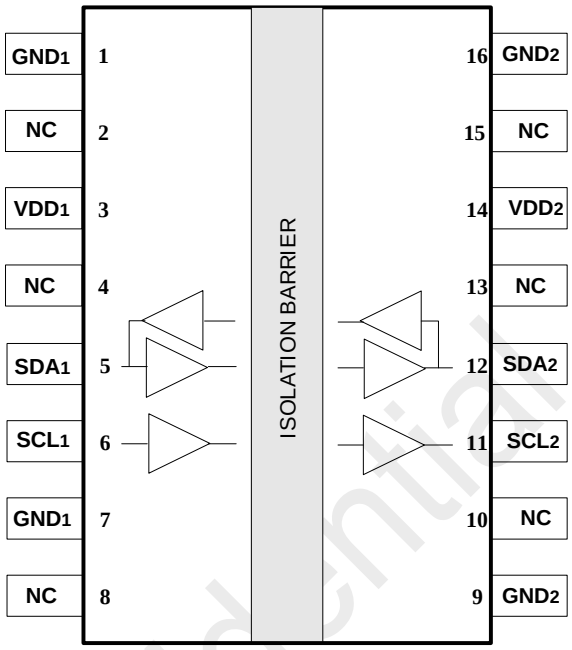


Figure 4. CMT8101W Pin List

Pin #	Pin Name	I/O	Description
1	GND1	-	Ground 1, the ground reference for Isolator Side 1
2	NC	-	No Connection.
3	VDD1	-	Power Supply for Isolator Side 1.
4	NC	-	No Connection.
5	SDA1	I/O	Serial data input /output, Side 1.
6	SCL1	I/O	Serial clock input /output, Side 1.
7	GND1	I/O	Ground 1, the ground reference for Isolator Side 1.
8	NC	-	No Connection.
9	GND2	-	Ground 2, the ground reference for Isolator Side 2.
10	NC	-	No Connection.
11	SCL2	I/O	Serial clock input /output, Side 2.
12	SDA2	I/O	Serial data input /output, Side 2.
13	NC	-	No Connection.
14	VDD2	-	Power Supply for Isolator Side 2.
15	NC	-	No Connection.
16	GND2	-	Ground 2, the ground reference for Isolator Side 2.

3 Typical Application

3.1 Typical Application Schematic

3.2 PCB Layout Guidelines

The CMT810x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. The figure below shows the recommended PCB layout. Make sure the space under the chip should keep free from planes, traces, pads and via. The pull-up resistors are required for both side 1 and side 2 buses. And the value of the resistors depends on the number of I2C devices on the bus.

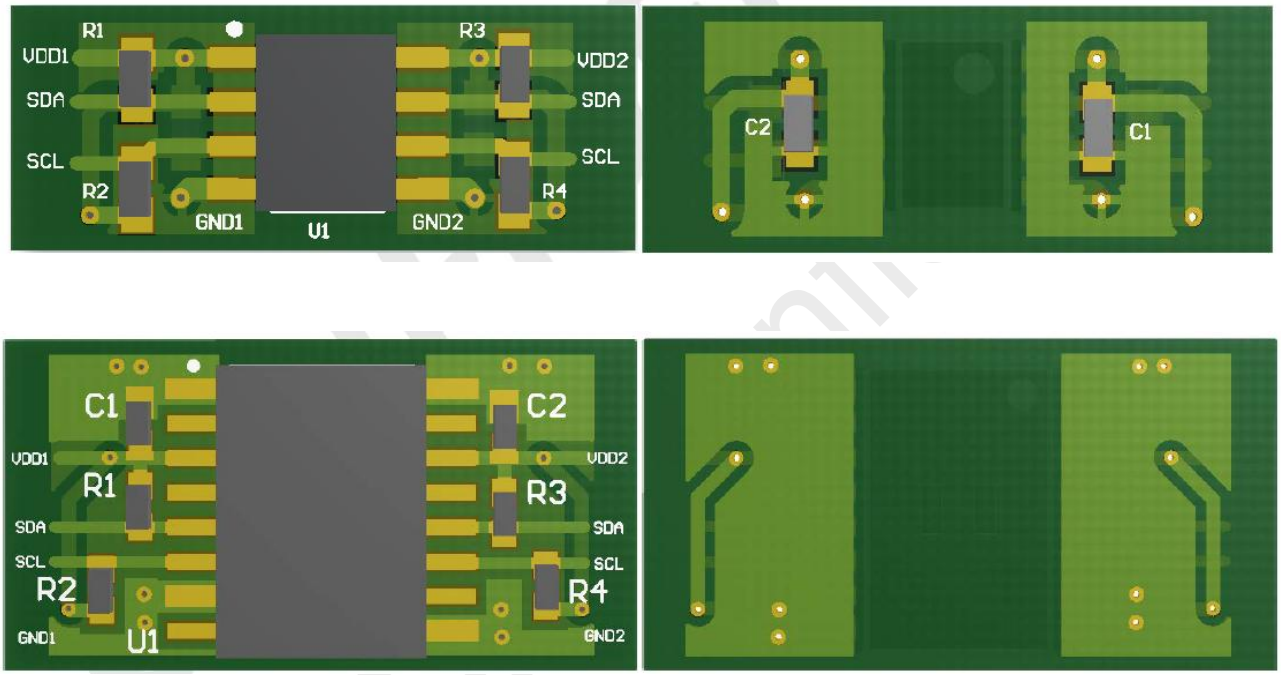


Figure 5. Recommended PCB Layout

4 Specifications

VDD1 = 2.5 ~ 5.5 V, VDD2 = 2.5 ~ 5.5 V, Ta = -40℃ to 125℃. Unless otherwise noted, typical values are at VDD1 = 5 V, VDD2 = 5 V, Ta = 25℃.

4.1 Electrical Characteristics

Table 3. Electrical Characteristics

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Power on reset	VDD_{POR}	POR threshold as during power-up		2.2		V
	VDD_{HYS}	POR threshold Hysteresis		0.1		V
Start up time after POR	trbs			40		usec
Common mode transient immunity	CMTI		±100		±150	kV/us

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Side 1 logic level						
Input threshold	V_{ILT1}	Input threshold at rising edge	400			mV
	V_{IHT1}				600	mV
	V_{IT_HYS1}	Input threshold hysteresis		100		mV
Low level output voltage	V_{OL1}	IOL ≤ 4mA，RPULL UP=1K	650		800	mV
Low-level output voltage to high-level input voltage threshold difference	ΔV_{OIT1}		70			mV
Side 2 Logic Level						
Input threshold	V_{ILT2}	Input threshold at rising edge		1.6		V
	V_{IT_HYS2}	Input threshold hysteresis		0.4		V
High level input voltage	V_{IH2}		2.0			V
Low level input voltage	V_{IL2}				0.8	V
Low level output voltage	V_{OL}	IOL ≤ 30mA			0.5	V

4.2 Supply Current Characteristics with 5 V Supply

VDD1 = 5 V ± 10%, VDD2 = 5 V ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 5 V, VDD2 = 5 V, Ta = 25 ℃.

Table 4. Supply Current Characteristics with 5 V Supply

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CMT8100						
Supply current All Input 0 V	I_{DD1}(Q0)			5.10	7.5	mA
	I_{DD2}(Q0)			3.96	5.7	mA
Supply current: All Input at supply	I_{DD1}(Q1)			2.52	3.6	mA
	I_{DD2}(Q1)			1.78	2.5	mA
Supply current: All Input with 2MHz, C_L=15pF	I_{DD1}(2M)			3.83	5.7	mA
	I_{DD2}(2M)			2.78	4.2	mA
CMT8101						
Supply current All Input 0V	I_{DD1}			4.08	6.12	mA
	I_{DD2}			2.81	4.22	mA
Supply current: All Input at supply,	I_{DD1}			1.6	2.4	mA
	I_{DD2}			1.69	2.54	mA
Supply current: All Input with 2MHz, C_L=15pF	I_{DD1}			2.65	3.98	mA
	I_{DD2}			4	6	mA
Clock rate	DR		0		2	MHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay	t_{PLH12}	See figure.6, R1=1500Ω, R2=500Ω, no load		24.8	37.2	ns
	t_{PHL12}	See figure.6, R1=1500Ω, R2=500Ω, no load		32.8	49.2	ns
	t_{PLH21}	See figure.6, R1=1500Ω, R2=500Ω, no load		24	36	ns
	t_{PHL21}	See figure.6, R1=1500Ω, R2=500Ω, no load		38	57	ns
Pulse width distortion	PWD_{12}	$\lvert t_{PHL12} - t_{PLH12} \rvert$		8	12	ns
	PWD_{21}	$\lvert t_{PHL21} - t_{PLH21} \rvert$		14	21	ns
Falling time	t_{f1}	C_L = 30pF		10.6	15.9	ns
	t_{f2}	C_L = 300pF		22.8	34.2	ns

4.3 Supply Current Characteristics with 3.3 V Supply

VDD1 = 3.3 V ± 10%, VDD2 = 5 V ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 3.3 V, VDD2 = 3.3 V, Ta = 25 ℃.

Table 5. Supply Current Characteristics with 3.3 V Supply

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CMT8100						
Supply current All Input 0V	I_{DD1}(Q0)			4.96	7.4	mA
	I_{DD2}(Q0)			3.85	5.6	mA
Supply current: All Input at supply,	I_{DD1}(Q1)			2.40	3.5	mA
	I_{DD2}(Q1)			1.68	2.4	mA
Supply current: All Input with 2MHz, C_L=15pF	I_{DD1}(2M)			3.69	5.6	mA
	I_{DD2}(2M)			2.67	4.2	mA
CMT8101						
Supply current All Input 0V	I_{DD1}			4	6	mA
	I_{DD2}			2.72	4.08	mA
Supply current: All Input at supply,	I_{DD1}			1.53	2.3	mA
	I_{DD2}			1.61	2.42	mA
Supply current: All Input with 2MHz, C_L=15pF	I_{DD1}			2.68	4.02	mA
	I_{DD2}			3.48	5.22	mA
Clock rate	DR		0		2	MHz
Propagation delay	t_{PLH12}	See figure.6, R1=1500Ω, R2=500Ω, no load		24.8	37.2	ns
	t_{PHL12}	See figure.6, R1=1500Ω, R2=500Ω, no load		32.8	49.2	ns

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	t_{PLH21}	See figure.6, R1=1500Ω, R2=500Ω, no load		24	36	ns
	t_{PHL21}	See figure.6, R1=1500Ω, R2=500Ω, no load		38	57	ns
Pulse width distortion	PWD_{12}	$\lvert t_{PHL12} - t_{PLH12} \rvert$		8	12	ns
	PWD_{21}	$\lvert t_{PHL21} - t_{PLH21} \rvert$		14	21	ns
Falling time	t_{f1}	CL = 30pF		10.6	15.9	ns
	t_{f2}	CL = 300pF		22.8	34.2	ns

4.4 Supply Current Characteristics with 2.5 V Supply

VDD1 = 2.5 V ± 10%, VDD2 = 2.5 ± 10%, Ta = -40 ℃ to 125 ℃. Unless otherwise noted, Typical values are at VDD1 = 2.5 V, VDD2 = 2.5 V, Ta = 25 ℃.

Table 6. Supply Current Characteristics with 2.5 V Supply

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CMT8100						
Supply current All Input 0V	$I_{DD1}(Q0)$			4.89	7.3	mA
	$I_{DD2}(Q0)$			3.79	5.5	mA
Supply current: All Input at supply,	$I_{DD1}(Q1)$			2.34	3.4	mA
	$I_{DD2}(Q1)$			1.63	2.3	mA
Supply current: All Input with 2MHz, C_L=15pF	$I_{DD1}(2M)$			3.61	5.4	mA
	$I_{DD2}(2M)$			2.59	4	mA
CMT8101						
Supply current All Input 0V	I_{DD1}			3.95	5.93	mA
	I_{DD2}			2.67	4.01	mA
Supply current: All Input at supply,	I_{DD1}			1.5	2.25	mA
	I_{DD2}			1.57	2.36	mA
Supply current: All Input with 2MHz, C_L=15pF	I_{DD1}			2.81	4.21	mA
	I_{DD2}			2.86	4.28	mA
Clock rate	DR		0		2	MHz
Propagation delay	t_{PLH12}	See figure 6, R1=1500Ω, R2=500Ω, no load		33	49.5	ns
	t_{PHL12}	See figure.6, R1=1500Ω, R2=500Ω, no load		52	78	ns
	t_{PLH21}	See figure.6, R1=1500Ω, R2=500Ω, no load		47	70.5	ns
	t_{PHL21}	See figure.6, R1=1500Ω, R2=500Ω, no load		100	150	ns

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Pulse width distortion	PWD_{12}	$\lvert t_{PHL12} - t_{PLH12} \rvert$		19	28.5	ns
	PWD_{21}	$\lvert t_{PHL21} - t_{PLH21} \rvert$		53	79.5	ns
Falling time	t_{f1}	C_L = 30pF		22	33	ns
	t_{f2}	C_L = 300pF		36	54	ns

4.5 Typical Characteristics

4.6 Parameter Measurement Circuit Setup

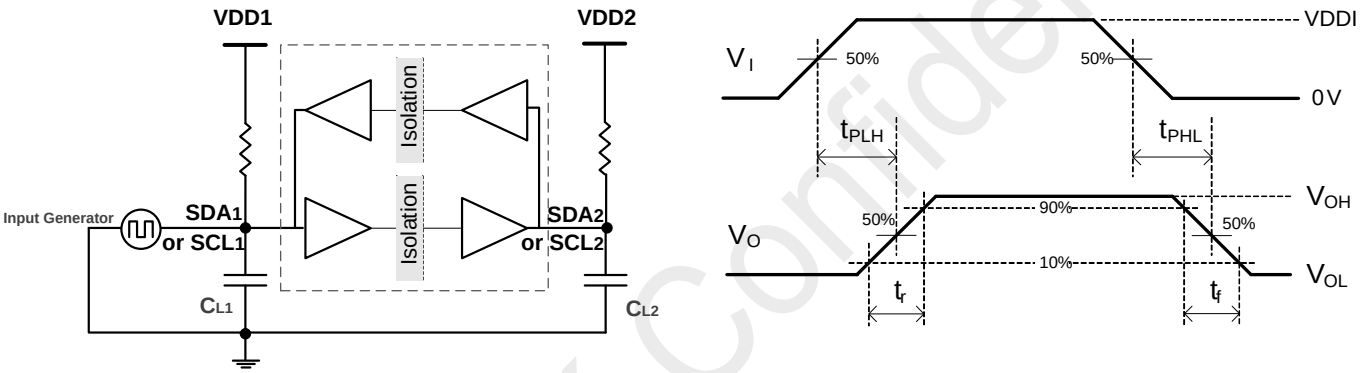


Figure 6. Switching Characteristic Test Circuit and Voltage Waveforms

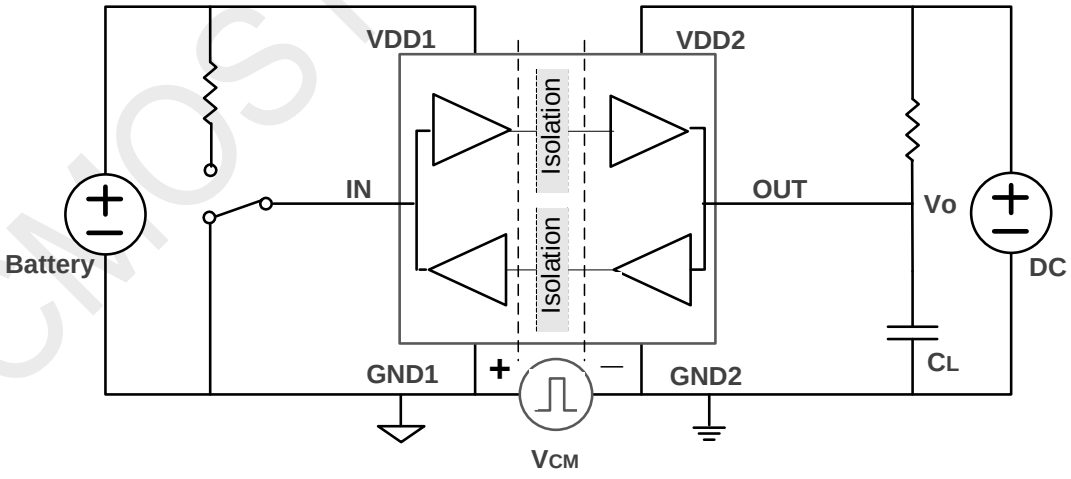


Figure 7. Common-Mode Transient Immunity Test Circuit

5 High Voltage Feature Specifications

5.1 Insulation and Safety Related Specifications

Table 7. Insulation and Safety Related Specifications

Parameter	Symbol	Condition	Value		Unit
			SOIC-8	SOIC-16	
Minimum External Air Gap (Clearance)	L(I01)	Shortest terminal-to-terminal distance through air	4.0	8.0	mm
Minimum External Tracking (Creepage)	L(I02)	Shortest terminal-to-terminal distance across the package surface	4.0	8.0	mm
Minimum internal gap	DTI	Distance through insulation	20		um
Tracking Resistance(Comparative Tracking Index)	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	>400		V
Material Group			Ⅱ		

5.2 DIN VDE V 0884-11(VDE V 0884-11):2017-01 Insulation Characteristics

Table 8. DIN VDE V 0884-11(VDE V 0884-11):2017-01 Insulation Characteristics

Description	Symbol	Test Condition	Value		Unit
			SOIC-8	SOIC-16	
Installation classification per DIN VDE 0110					
For rated mains voltage ≤ 150 V_{rms}			Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For rated mains voltage ≤ 300 V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
For rated mains voltage ≤ 400 V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	
Climatic classification			10/105/21	10/105/21	
Pollution degree per DIN VDE 0110, table 1			2	2	
Maximum repetitive isolation voltage	V_{IORM}		565	849	Vpeak
Input to output test voltage, method B1	$V_{pd(m)}$	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	847	1273	Vpeak
Input to output test voltage, method A					
After environmental tests subgroup 1	$V_{pd(m)}$	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	678	1019	Vpeak
After Input and /or safety test subgroup 2 and subgroup 3	$V_{pd(m)}$	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	678	1019	Vpeak
Maximum transient isolation voltage	V_{IOTM}	t = 60 sec	5300	7000	Vpeak

Maximum surge isolation voltage	V_{IOSM}	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.3\times V_{IOSM}$	5384	5384	Vpeak
Isolation resistance	R_{IO}	V_{IO} =500V	$>10^9$	$>10^9$	Ω
Isolation capacitance	C_{IO}	f = 1MHz	0.6	0.6	pF
Input capacitance	C_I		2	2	pF
Total power dissipation at 25℃	Ps			1499	mW
Safety input, output, or supply current	Is	θ_{JA} = 140 °C/W, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	160		mA
		θ_{JA} = 84 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C		237	mA
Case temperature	Ts		150	150	℃

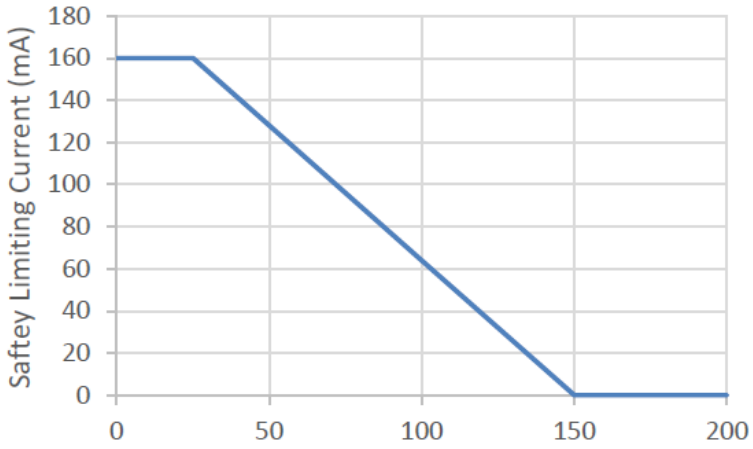


Figure 8. CMT8100N/8101N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

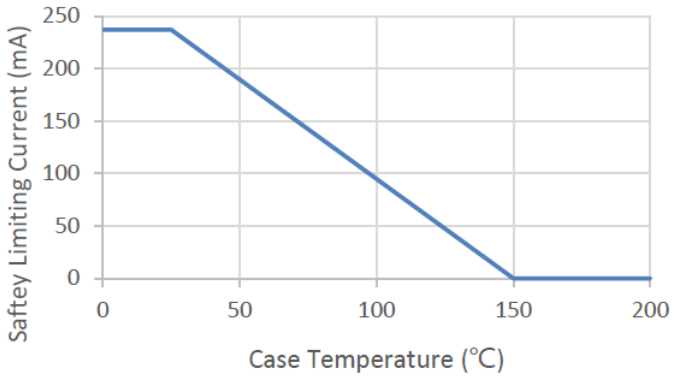


Figure 9. CMT8100W/8101W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

5.3 Regulation Information

The CMT8100N/CMT8101N are approved by the organizations listed in table below.

Table 9. CMT8100N/CMT8101N Regulation Conformation

CUL		VDE	CQC
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01 [2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750 Vrms Isolation voltage	Single Protection, 3750 Vrms Isolation voltage	Basic Insulation 565 Vpeak, VIOSM=5384Vpeak	Basic insulation at 400 Vrms (565 Vpeak)
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)
[1]. In accordance with UL 1577, each NSi8100N/NSi8101N is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec. [2]. In accordance with DIN VDE V 0884-11, each NSi8100N/NSi8101N is proof tested by applying an insulation test voltage ≥ 847 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11.			

The CMT8100W/CMT8101W are approved by the organizations listed in table below.

Table 10. CMT8100WCMT8101 Regulation Conformation

CUL		VDE	CQC
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-012	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000 Vrms Isolation voltage	Single Protection, 5000 Vrms Isolation voltage	Basic Insulation 849Vpeak, VIOSM=5384Vpeak	Basic insulation at 800 Vrms (1131Vpeak) Reinforced insulation at 400Vrms (565Vpeak)
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)
[1]. In accordance with UL 1577, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ⩾ 6000 V rms for 1 sec. [2]. In accordance with DIN VDE V 0884-11, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ⩾ 1273 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.			

6 Function Description

6.1 Function Overview

The CMT810x is a bidirectional isolator based on a capacitive isolation barrier technique. The CMT810x devices are compatible with I2C interface. Internally, the I2C interface is split into two unidirectional channels communicating in opposite directions via a dedicate capacitive isolation channel for each. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The CMT8100 devices are high reliability dual-channel bidirectional isolators for clock and data lines while CMT8101 has a bidirectional data and a unidirectional clock channel. The CMT8100 is suitable for multi-master application while CMT8101 is useful in a single master application.

The side 2 logic levels of CMT810x are standard I2C value, and the maximum load for side 2 is $\leqslant$ 400 pF. So multiple CMT810x devices connected to a bus by their Side 2 pins can communicate with each other and with other I2C compatible devices.

The side 1 logic levels of CMT810x are not standard value. The output low level of CMT810x is 650mV, while low-level output voltage to high-level input voltage threshold is 50 mV. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I2C bus.

The CMT810x devices are AEC-Q100 qualified. The CMT810x device is safety certified by UL1577 support several insulation withstand voltages (3.75 kVrms, 5 kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I2C clock of the CMT810x is up to 2 MHz, and the common-mode transient immunity (CMTI) is up to 150 kV/us. Wide supply voltage of the CMT810x device supports to connect with most digital interfaces directly, easy to do the level shift. High system level EMC performance enhances reliability and stability.

The table below shows the functional status of CMT810x. The CMT810x is high impedance output when VDDIN is unready and VDDOUT is ready as shown in the table below.

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Table 11. Output Status vs. Power Status

Input	VDD1 Status	VDD2 Status	Output	Comment
H	Ready	Ready	Z	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	Z	The output follows the same status with the input within 60 us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60 us after output side VDD2 is powered on.

7 Packaging Information

The packaging information of the CMT810x is shown in the figures below.

7.1 CMT8100N/CMT8101N Narrow Body SOIC-8 Packaging

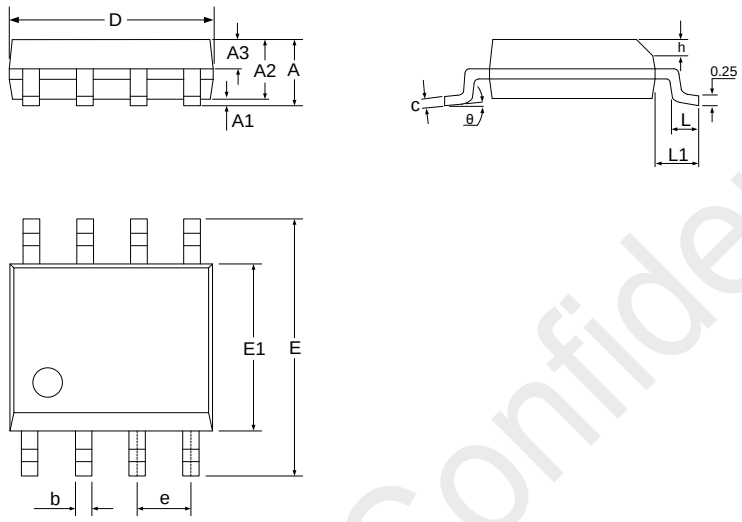


Figure 10. Narrow Body SOIC-8 Packaging

Table 12. Narrow Body SOIC-8 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.30	1.40	1.50
b	0.30	0.42	0.51
c	0.17	0.21	0.25
D	4.80	5.00	5.20
E1	3.90	4.00	4.10
E	5.80	6.10	6.20
e	1.27 BSC		
L	0.40	0.60	0.80
θ	0	-	8°

7.2 CMT8100W/CMT8101W Wide Body SOIC-16 Packaging

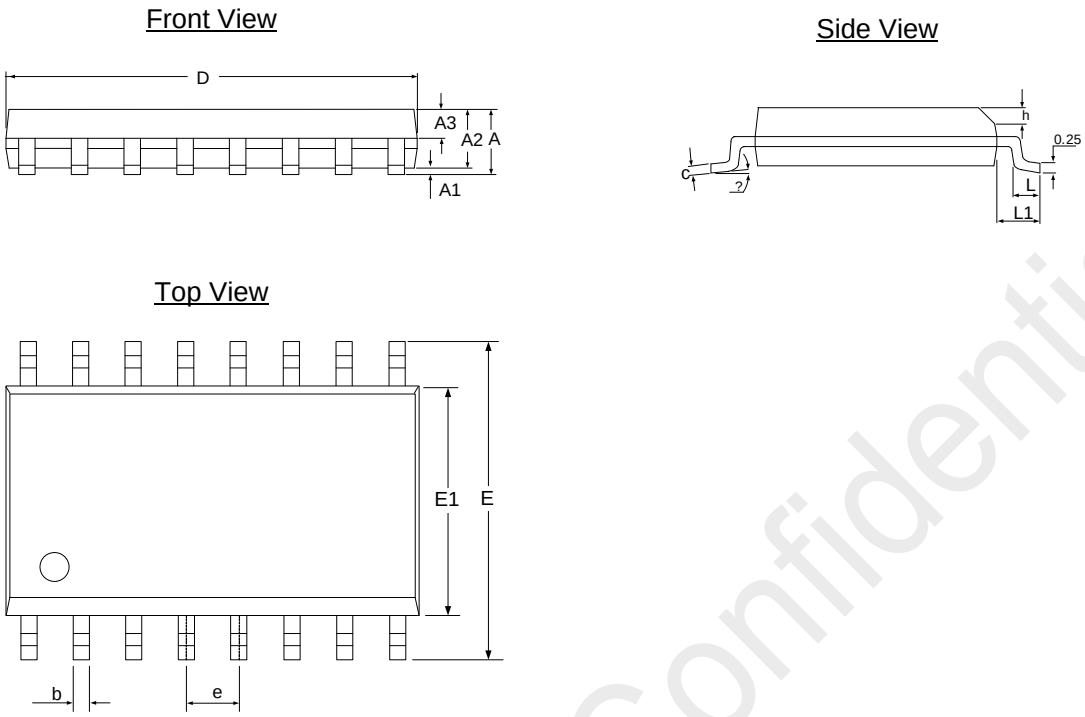


Figure 11. Wide Body SOIC-16 Packaging

Table 13. Wide Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1	1.40		
θ	0	-	8°

8 Top Marking

Figure 12. CMT810x Top Marking

Table 14. CMT810x Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.5 mm, align right
Line 1 Marking	P = 0 / 1 , refers to part number CMT8100x / CMT8101x respectively. NN is the last characters following CMT810P in part number naming. See Chapter 11 part number naming rule for details
Line 2 Marking	The date code is assigned by the package factory. YY is the last 2 digits of the year. WW is the working week. ①②③④⑤⑥ is internal trace code

9 Ordering Information

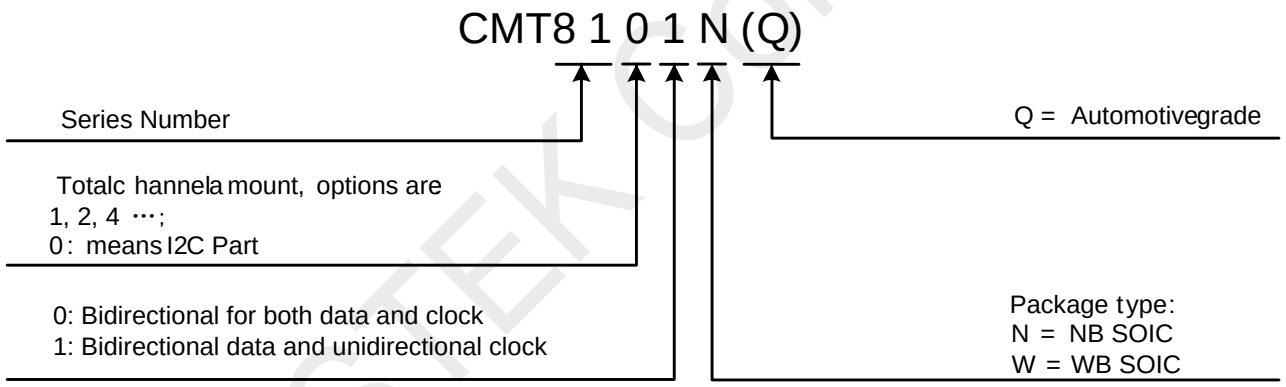
Table 15. Part Number List

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Clock Rate (MHz)	Temperature	Automotive	Package
CMT8100N	3.75	2	2	2	-40 to 125℃	NO	SOIC8
CMT8100NQ	3.75	2	2	2	-40 to 125℃	YES	SOIC8
CMT8101N	3.75	2	1	2	-40 to 125℃	NO	SOIC8
CMT8101NQ	3.75	2	1	2	-40 to 125℃	YES	SOIC8
CMT8100W	5	2	2	2	-40 to 125℃	NO	WB SOIC16
CMT8101W	5	2	1	2	-40 to 125℃	NO	WB SOIC16

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. All devices are AEC-Q100 qualified.

Part Number Naming Rule:



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Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

10 Revise History

Table 16. Revise History Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2021/11/02

11 Contacts

CMOSTEK Microelectronics Co., Ltd. Shenzhen Branch
Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-83231427
Post Code: 518055
Sales: sales@cmostek.com
Supports: support@cmostek.com
Website: www.cmostek.com