SNx4AHC08 Quadruple 2-Input Positive-AND Gates

1 Features

- 2-V to 5.5-V Operating Range
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Network Switches
- PCs and Notebooks
- Electronic Points of Sale

3 Description

The SNx4AHC08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC08	SOIC (14)	8.65 mm × 3.90 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TVSOP (14)	3.60 mm × 4.40 mm
	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm
SN54AHC08	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (May 2013) to Revision J — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision H (March 1996) to Revision I — **Page**

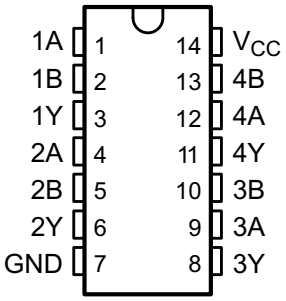
- Changed document format ... 1
- Extended operating temperature range to 125°C ... 5

5 Device Comparison Table

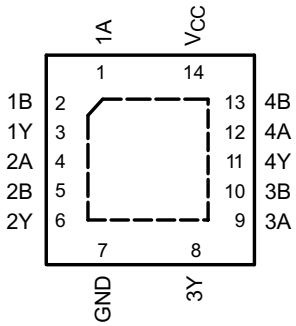
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC08D	SOIC (14)	8.65 mm × 3.90 mm
SN74AHC08DB	SSOP (14)	6.20 mm × 5.30 mm
SN74AHC08DGV	TVSOP (14)	3.60 mm × 4.40 mm
SN74AHC08N	PDIP (14)	19.30 mm × 6.35 mm
SN74AHC08NS	SO (14)	10.30 mm × 5.30 mm
SN74AHC08PW	TSSOP (14)	5.00 mm × 4.40 mm
SN74AHC08RGY	VQFN (14)	3.50 mm × 3.50 mm
SN54AHC08FK	LCCC (20)	8.89 mm × 8.89 mm

6 Pin Configuration and Functions

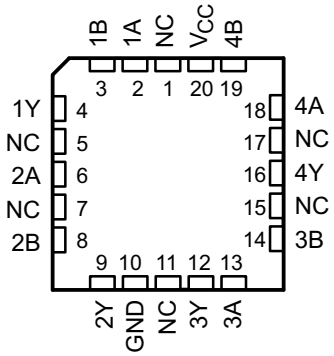
D, DB, DGV, N, NS, PW, or W Package
14-Pin SOIC, SSOP, TVSOP, PDIP, SO, or TSSOP
Top View



RGY Package
14-Pin VQFN
Top View



FK Package
20-Pin LCCC
Top View



NC – No internal connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, PDIP, SO, TSSOP	VQFN	LCCC		
1A	1	1	2	I	1A Input
1B	2	2	3	I	1B Input
1Y	3	3	4	O	1Y Output
2A	4	4	6	I	2A Input
2B	5	5	8	I	2B Input
2Y	6	6	9	O	2Y Output
3Y	8	8	12	O	3Y Output
3A	9	9	13	I	3A Input
3B	10	10	14	I	3B Input
4Y	11	11	16	O	4Y Output
4A	12	12	18	I	4A Input
4B	13	13	19	I	4B Input
GND	7	7	10	—	Ground Pin
NC	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V_{CC}	14	14	20	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage, V_O(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC}= 2 V	1.5		V
		V_{CC}= 3V	2.1		
		V_{CC}= 5.5 V	3.85		
V_{IL}	Low-level Input voltage	V_{CC}= 2 V		0.5	V
		V_{CC}= 3 V		0.9	
		V_{CC}= 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}= 2 V		–50	mA
		V_{CC}= 3.3 V ± 0.3 V		–4	
		V_{CC}= 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC}= 2 V		50	mA
		V_{CC}= 3.3 V ± 0.3 V		4	
		V_{CC}= 5 V ± 0.5 V		8	
Δt/Δv	Input Transition rise or fall rate	V_{CC}= 3.3 V ± 0.3 V		100	ns/V
		V_{CC}= 5 V ± 0.5 V		20	
T_A	Operating free-air temperature	SN54AHC08	–55	125	°C
		SN74AHC08	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		SN74AHC08							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	127	80	76	113	47	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		V
		3 V	2.9	3		
		4.5 V	4.4	4.5		
	I_{OH} = –4 mA	3 V	2.58			
	I_{OH} = –8 mA	4.5 V	3.94			
V_{OL}	I_{OL} = 50 µA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I_{OH} = 4 mA	3 V			0.36	
	I_{OH} = 8 mA	4.5 V			0.36	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2	µA
C_i	V_I = V_{CC} or GND	5 V		4	10	pF

7.6 Electrical Characteristics, T_A = –55°C to 125°C, SN54AHC08

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V	1.9		V
		3 V	2.9		
		4.5 V	4.4		
	I_{OH} = –4 mA	3 V	2.48		
	I_{OH} = –8 mA	4.5 V	3.8		
V_{OL}	I_{OL} = 50 µA	2 V		0.1	V
		3 V		0.1	
		4.5 V		0.1	
	I_{OH} = 4 mA	3 V		0.5	
	I_{OH} = 8 mA	4.5 V		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±1 (1)	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V		20	µA
C_i	V_I = V_{CC} or GND	5 V			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

7.7 Electrical Characteristics, T_A = –40°C to 125°C, SN74AHC08

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V		1.9		V
		3 V		2.9		
		4.5 V		4.4		
	I_{OH} = –4 mA	3 V		2.48		
	I_{OH} = –8 mA	4.5 V		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I_{OH} = 4 mA	3 V	T_A = –40°C to 85°C		0.44	
			T_A = –40°C to125°C Recommended		0.5	
	I_{OH} = 8 mA	4.5 V	T_A = –40°C to 85°C		0.44	
			T_A = –40°C to125°C Recommended		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
C_i	V_I = V_{CC} or GND	5 V	T_A = –40°C to 85°C		10	pF

7.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A or B	Y	C_L = 15 pF	T_A = 25°C		6.2 (1)	8.8 (1)	ns
				T_A = –55°C to 125°C, SN54AHC08		1 (1)	10.5 (1)	
				T_A = –40°C to 85°C, SN74AHC08		1	10.5	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	10.5	
t_{PLH}, t_{PHL}	A or B	Y	C_L = 50 pF	T_A = 25°C		8.7	12.3	ns
				T_A = –55°C to 125°C, SN54AHC08		1	14	
				T_A = –40°C to 85°C, SN74AHC08		1	14	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	14	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A or B	Y	C_L = 15 pF	T_A = 25°C		4.3(1)	5.9(1)	ns
				T_A = –55°C to 125°C, SN54AHC08		1(1)	7(1)	
				T_A = –40°C to 85°C, SN74AHC08		1	7	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	7	
t_{PLH}, t_{PHL}	A or B	Y	C_L = 50 pF	T_A = 25°C		5.8	7.9	ns
				T_A = –55°C to 125°C, SN54AHC08		1	9	
				T_A = –40°C to 85°C, SN74AHC08		1	9	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.10 Noise Characteristics, SN74AHC08

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

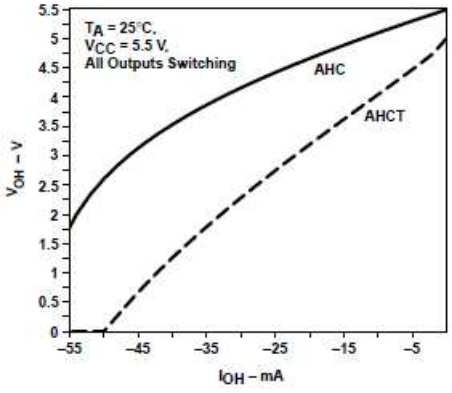
(1) Characteristics are for surface-mount packages only.

7.11 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

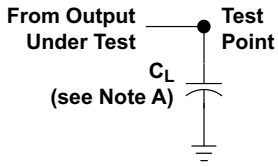
7.12 Typical Characteristics



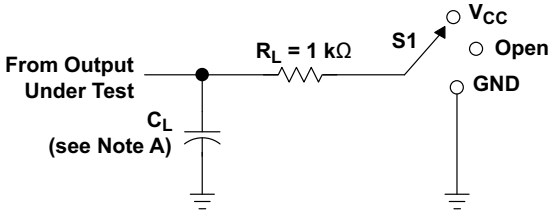
V_{CC} = 5.5 V

Figure 1. AHC Family V_{OL} vs I_{OL}

8 Parameter Measurement Information

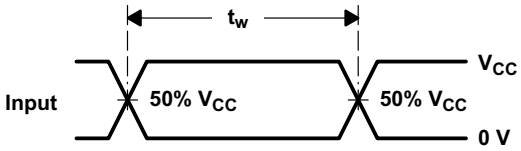


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

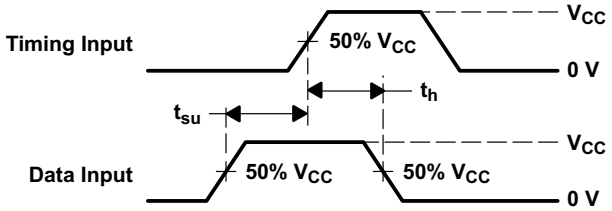


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

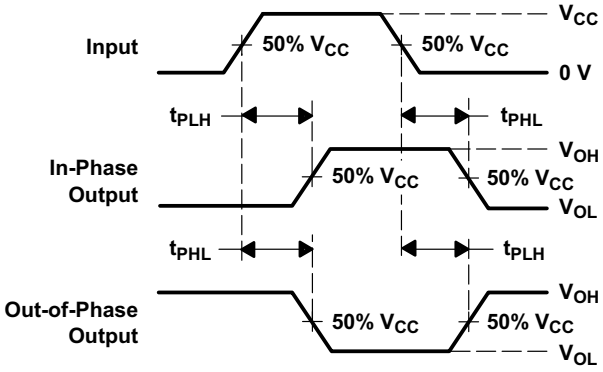
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



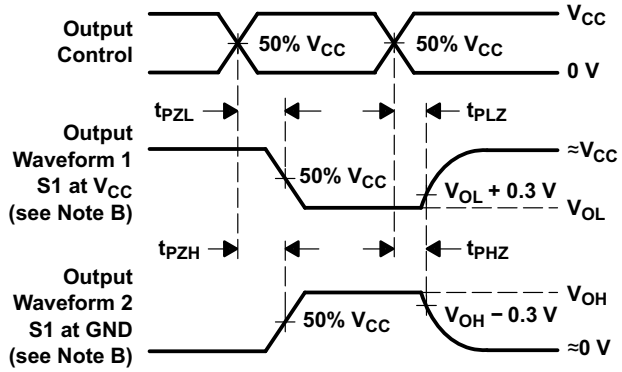
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4AHC08 devices are quadruple 2-input positive-AND gates with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The inputs are high impedance when V_{CC} = 0 V.

9.2 Functional Block Diagram

9.3 Feature Description

Slow rise and fall time on outputs allow for low-noise outputs.

9.4 Device Functional Modes

Table 1 is the function table for the SNx4AHC08.

Table 1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A common application for AND gates is the use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC08 to verify that the processor has turned on can protect it from harmful signals.

10.2 Typical Application

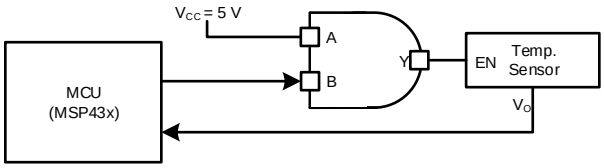


Figure 3. Typical Application Diagram

10.2.1 Design Requirements

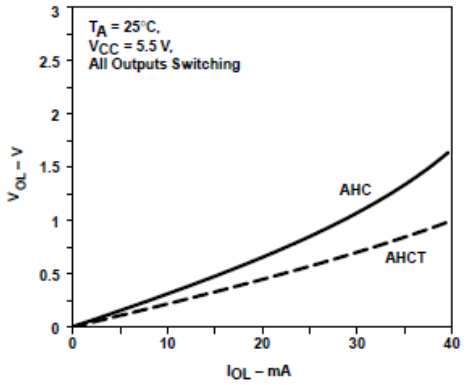
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/Δv) in the *Recommended Operating Conditions* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curve



V_{CC} = 5.5 V

Figure 4. AHC Family V_{OH} vs I_{OH}

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 5 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

12.2 Layout Example

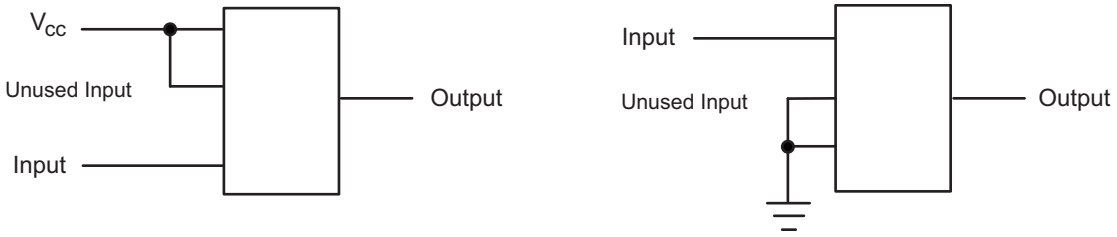


Figure 5. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC08	Click here	Click here	Click here	Click here	Click here
SN74AHC08	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9682001Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC 08FK	Samples
SN74AHC08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	Samples
SN74AHC08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	Samples
SN74AHC08DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	Samples
SN74AHC08DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	Samples
SN74AHC08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC08N	Samples
SN74AHC08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	Samples
SN74AHC08PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	Samples
SN74AHC08RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA08	Samples
SNJ54AHC08FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC 08FK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC08, SN74AHC08 :

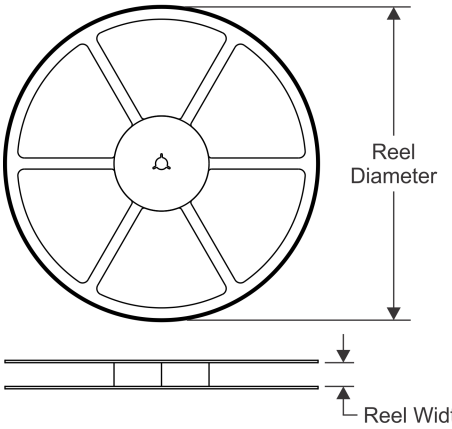
- Catalog : SN74AHC08
- Enhanced Product : SN74AHC08-EP, SN74AHC08-EP
- Military : SN54AHC08

NOTE: Qualified Version Definitions:

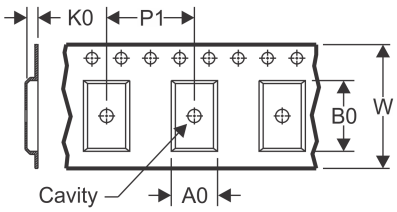
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

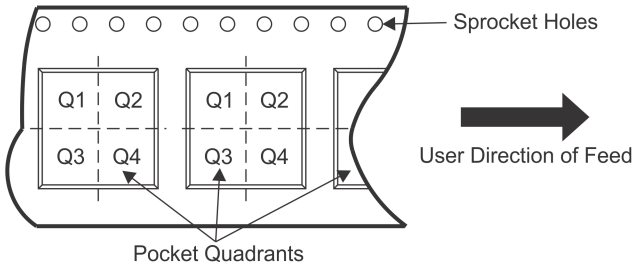


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

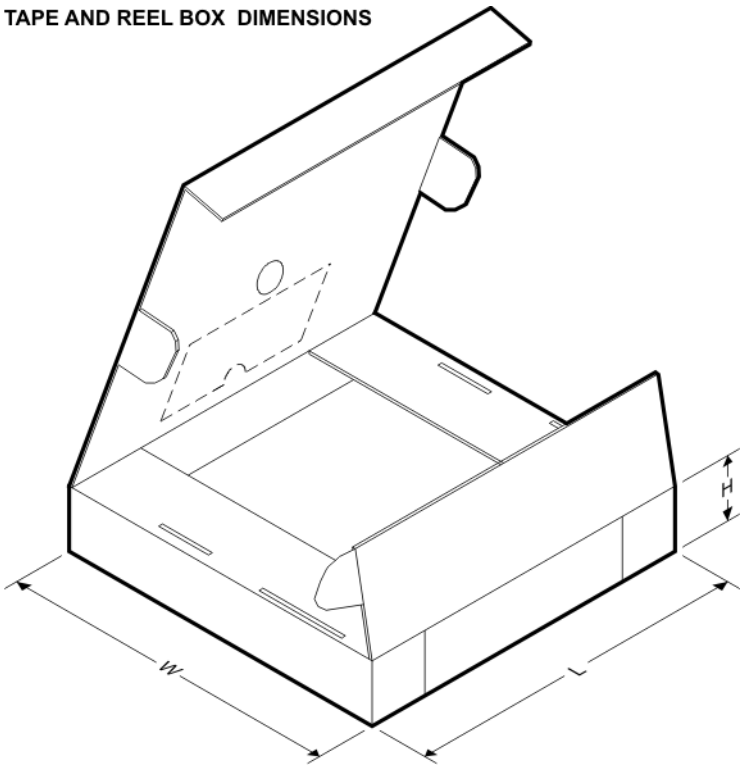
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC08DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC08NSR	SO	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

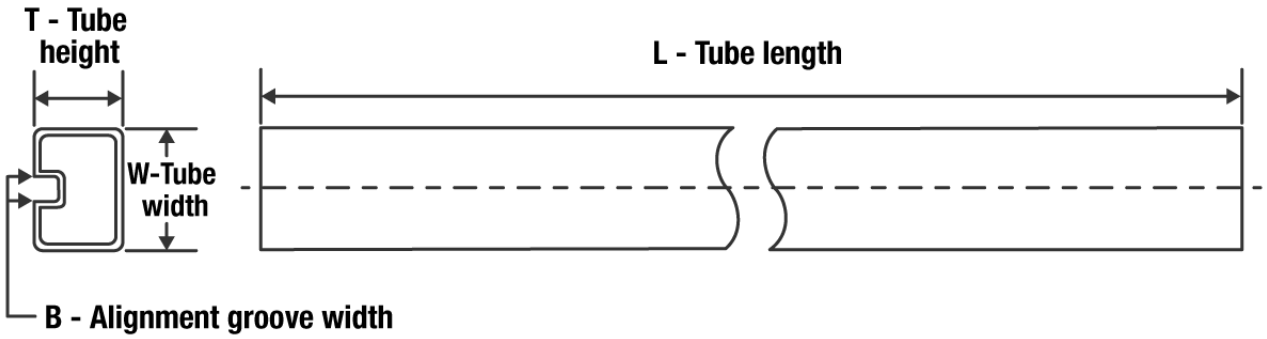
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC08DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74AHC08DGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74AHC08DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74AHC08NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74AHC08PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74AHC08PWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74AHC08PWRG4	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74AHC08RGYR	VQFN	RGY	14	3000	853.0	449.0	35.0

TUBE

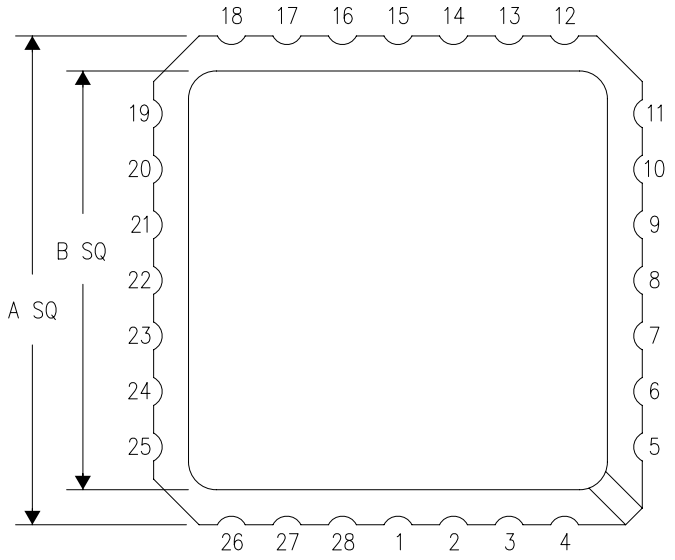


*All dimensions are nominal

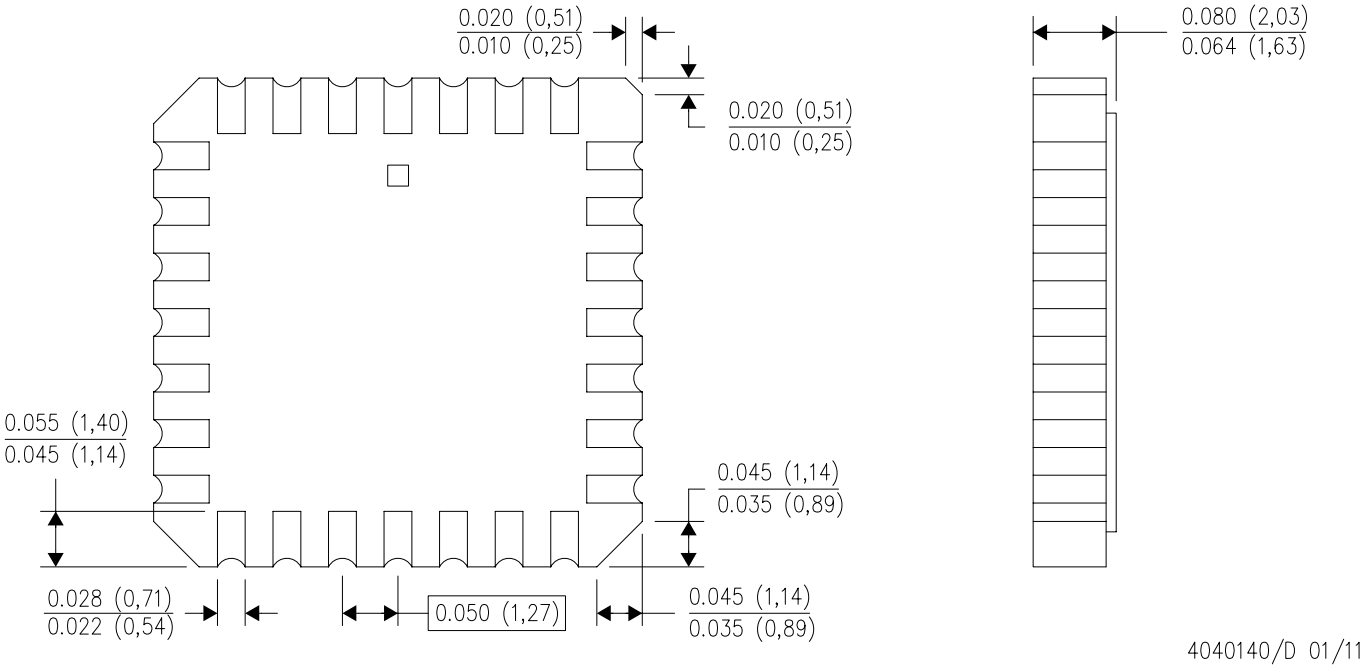
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9682001Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC08D	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC08DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74AHC08PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54AHC08FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



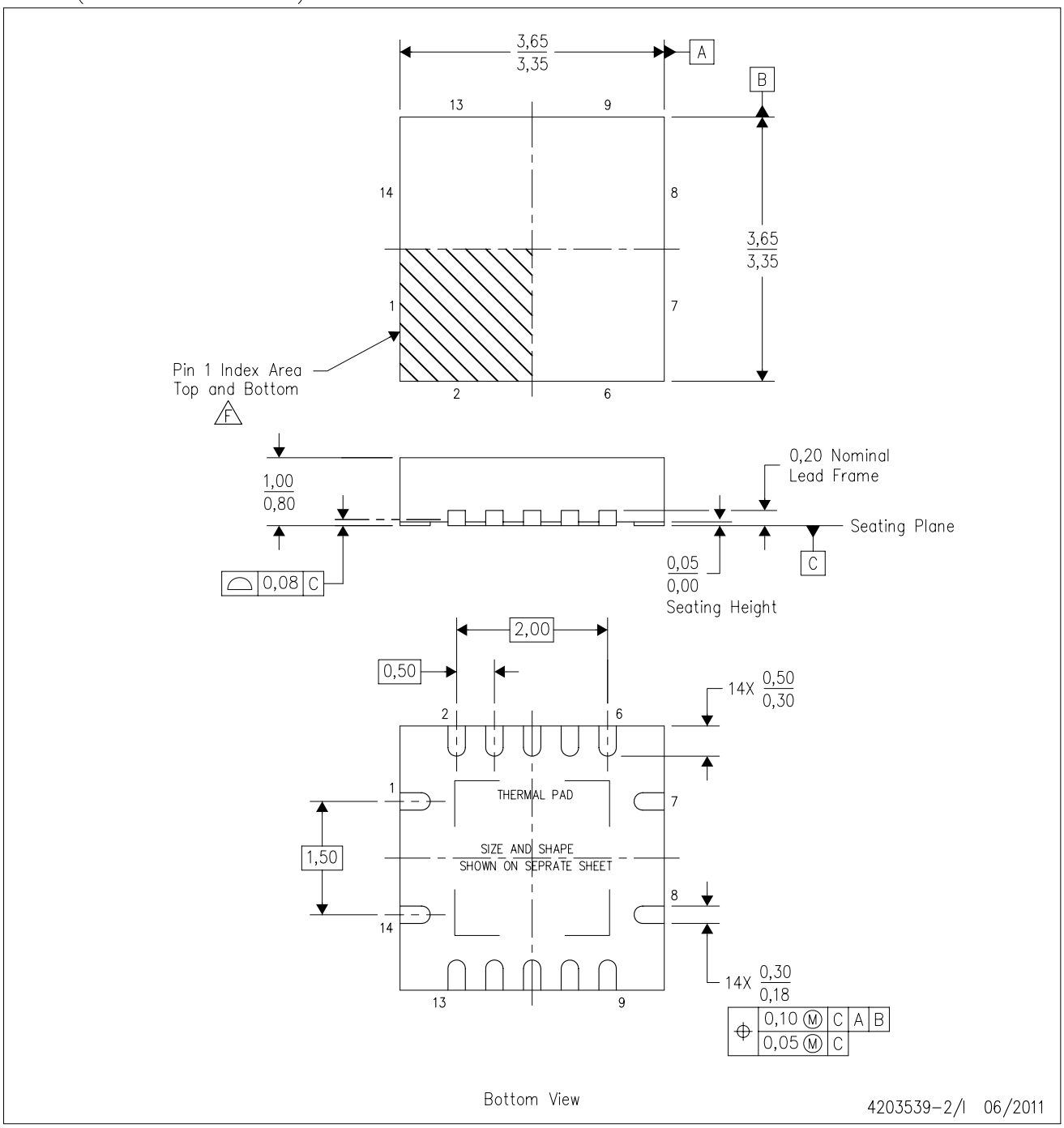
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

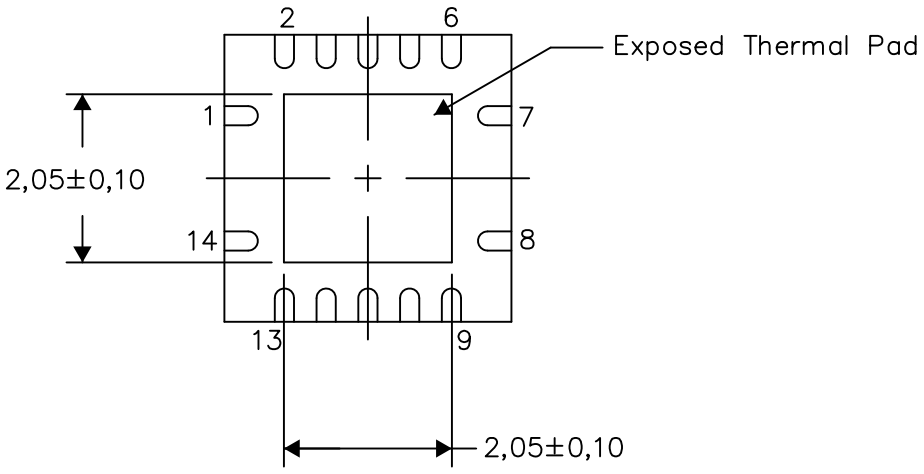
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



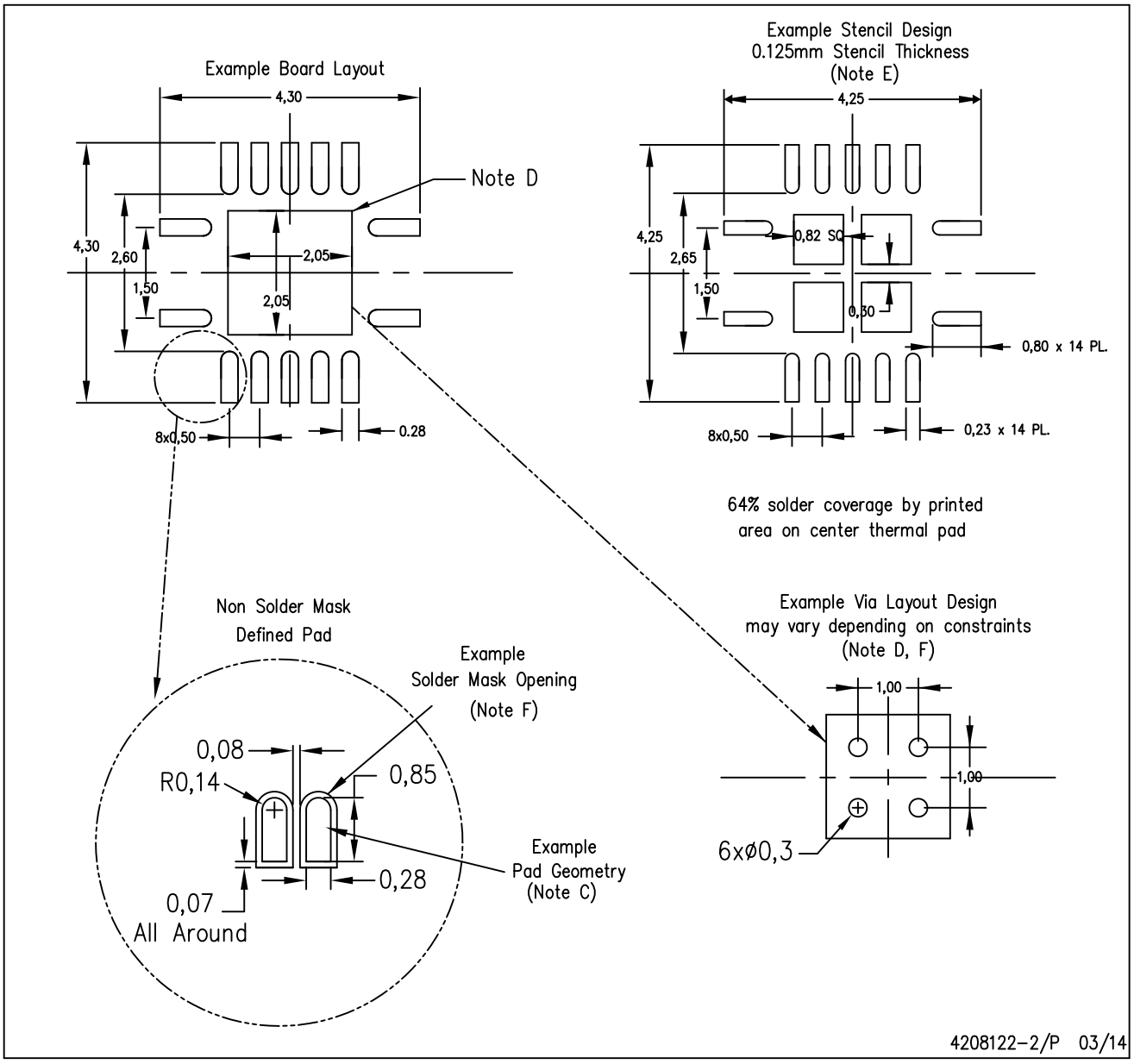
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

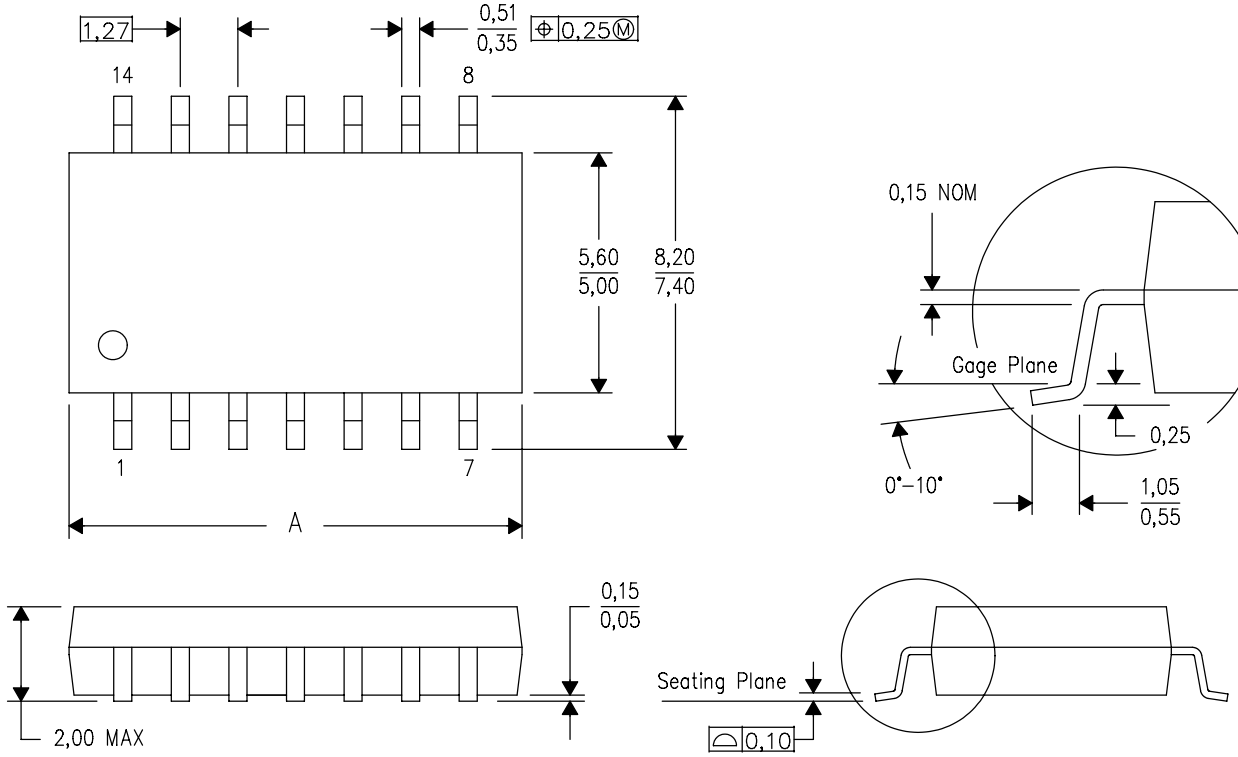


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



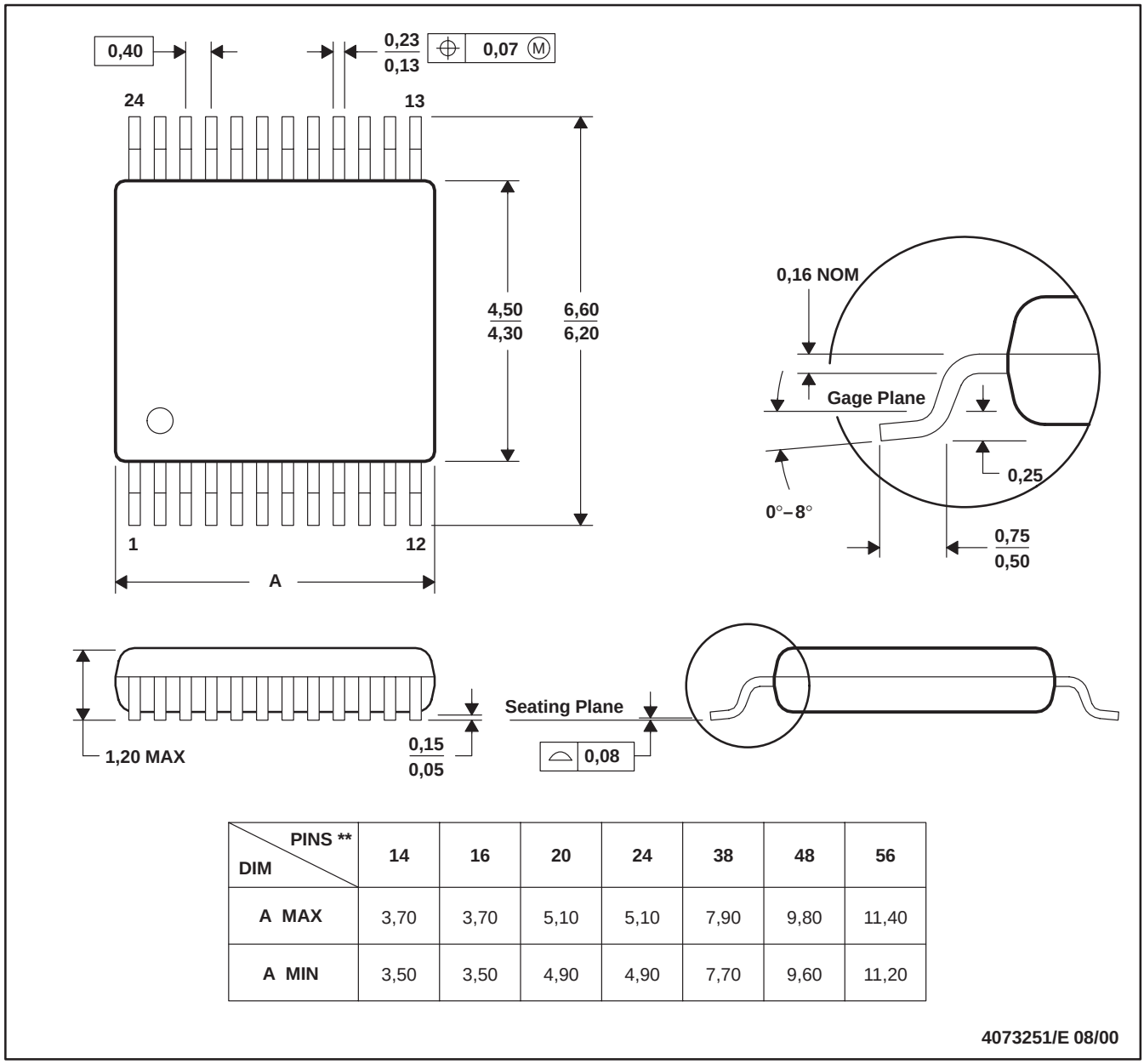
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

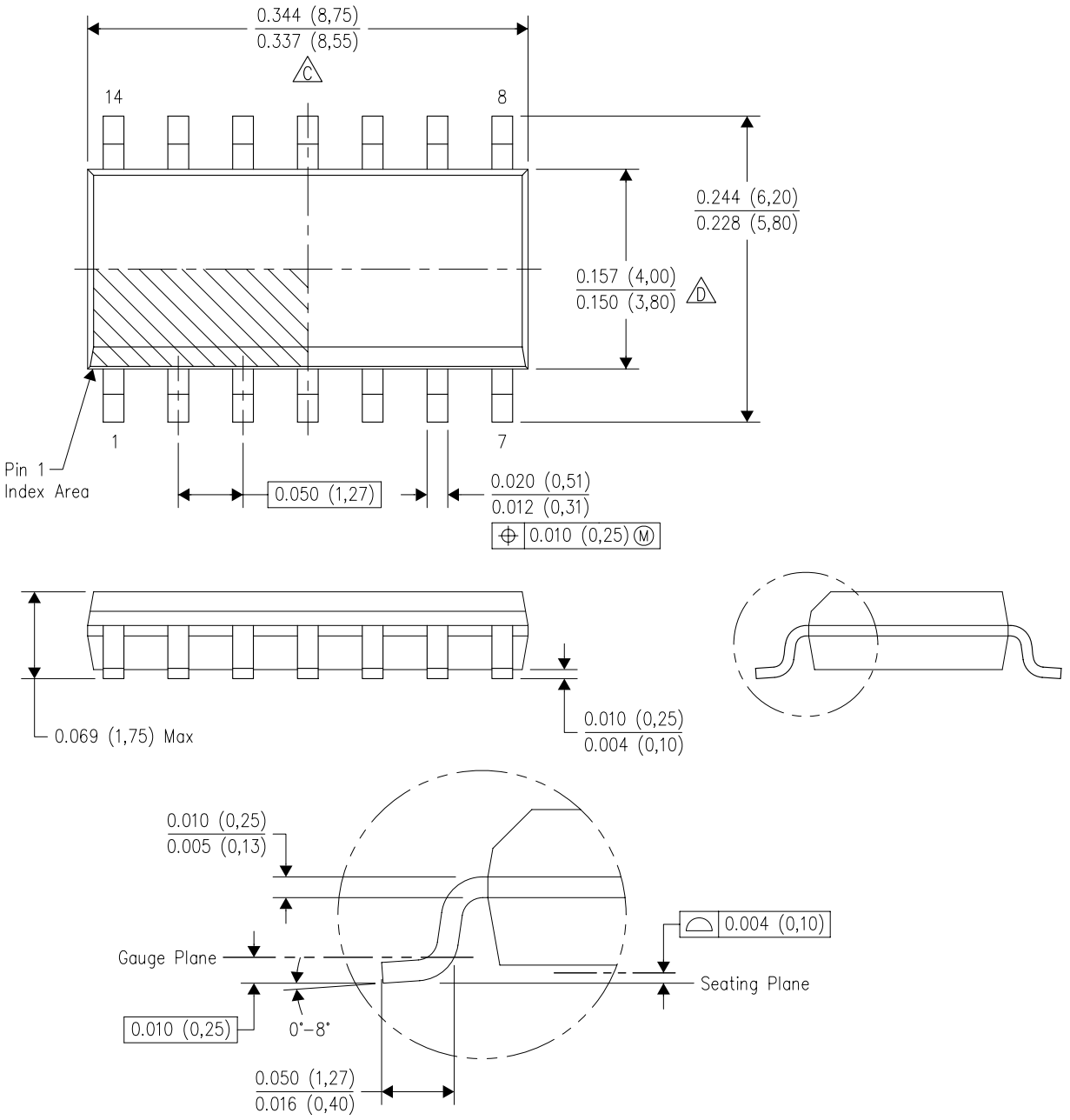


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

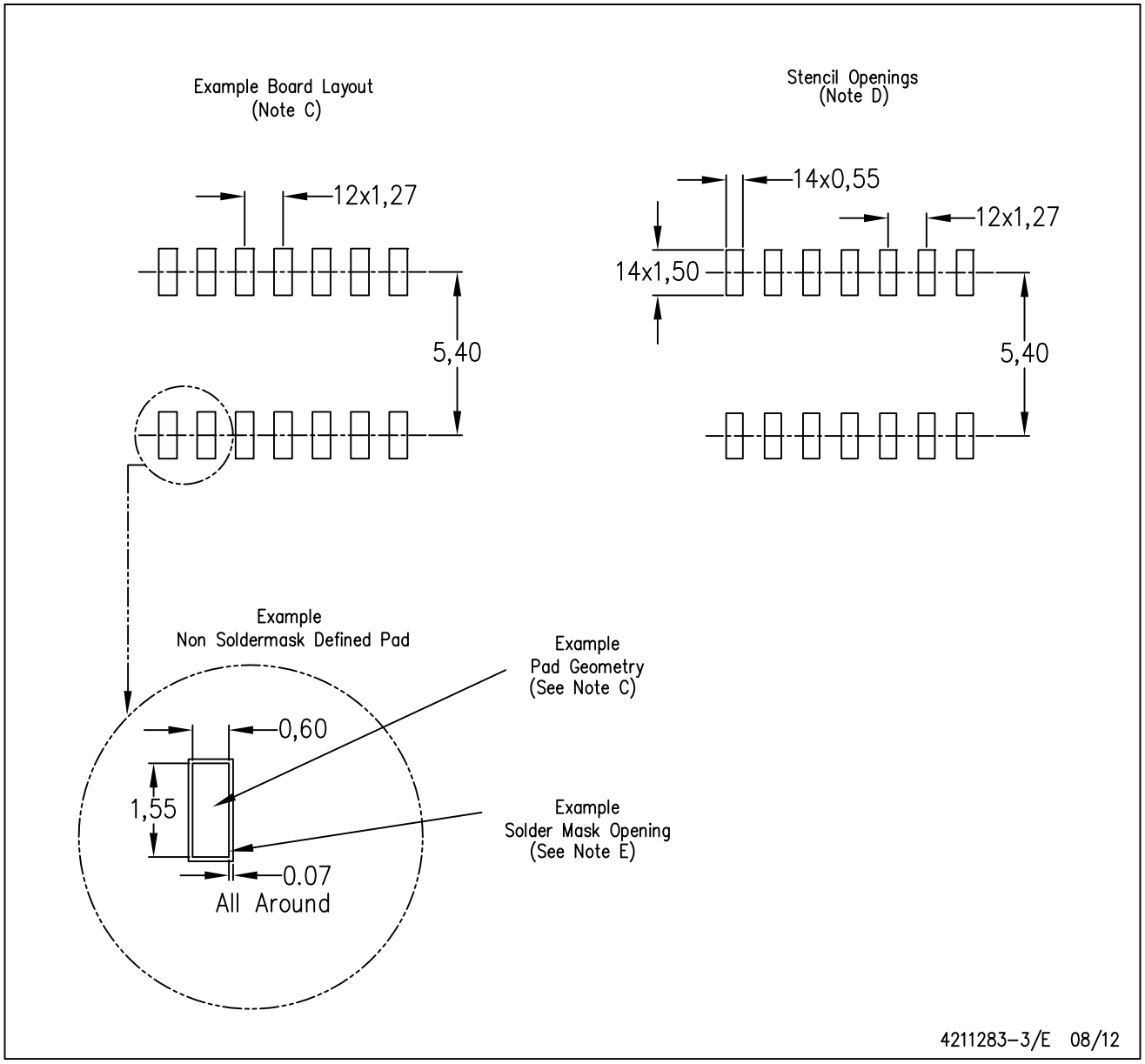
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

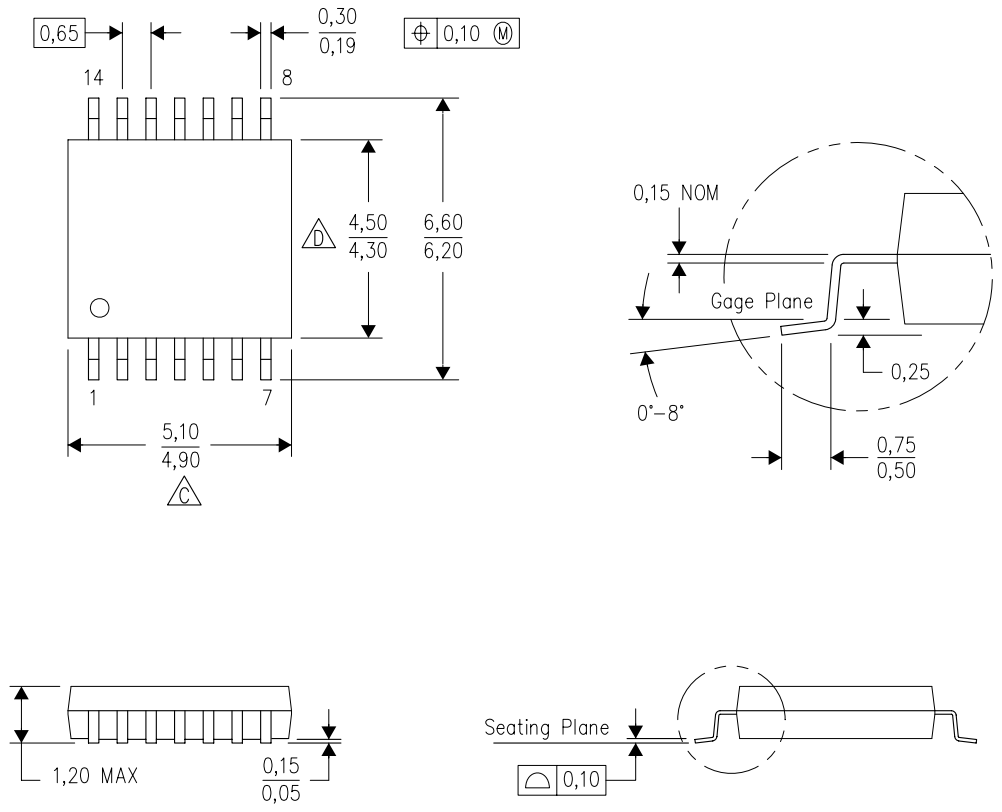
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

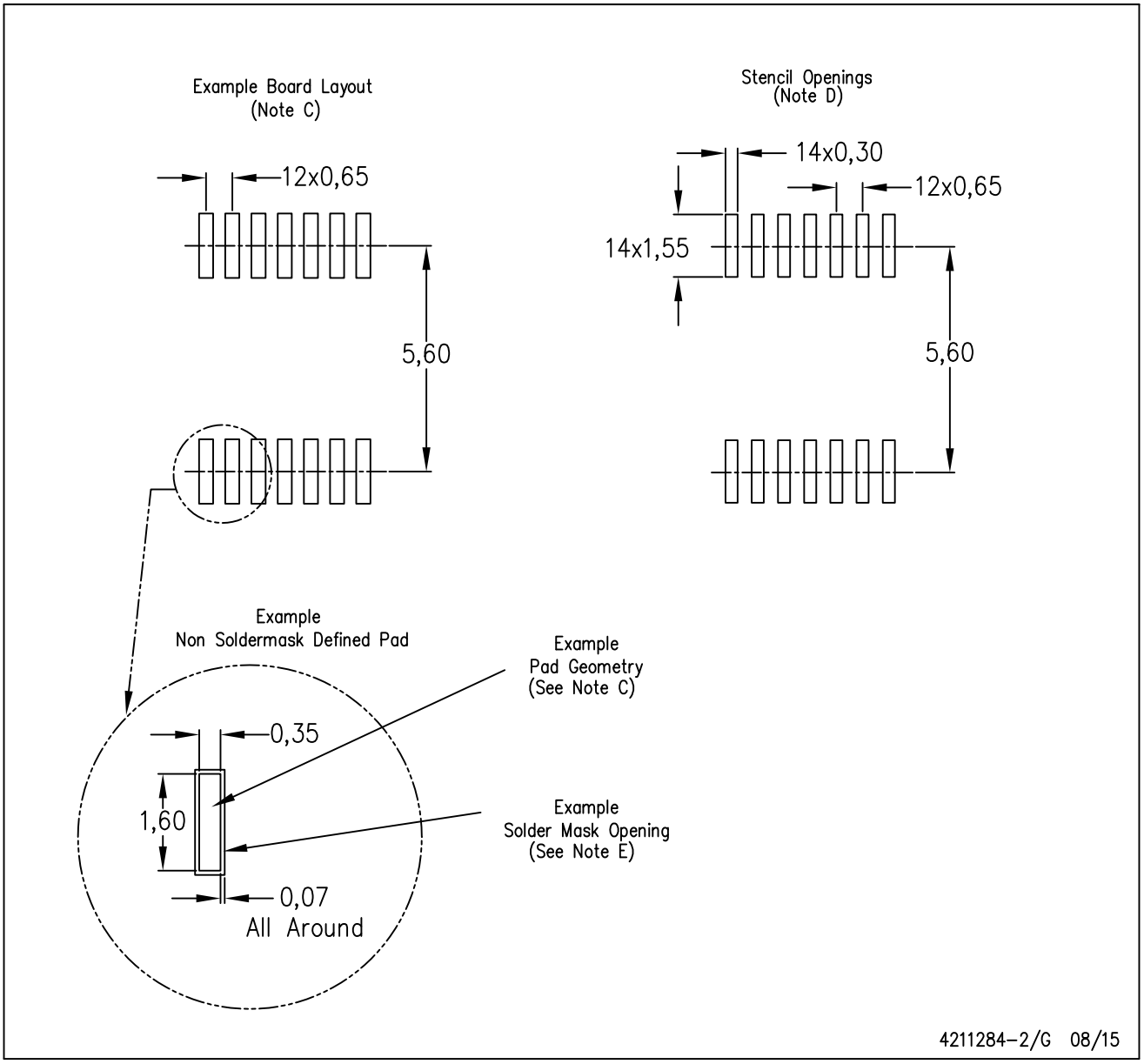
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

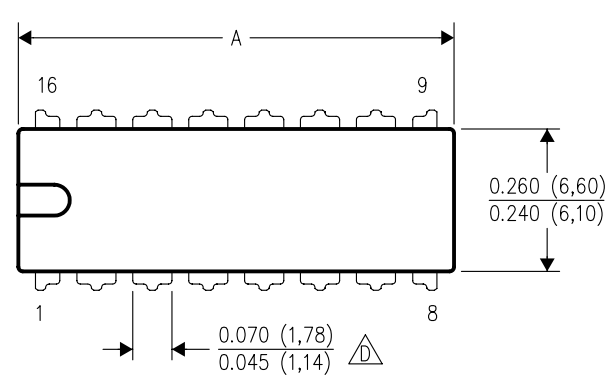


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

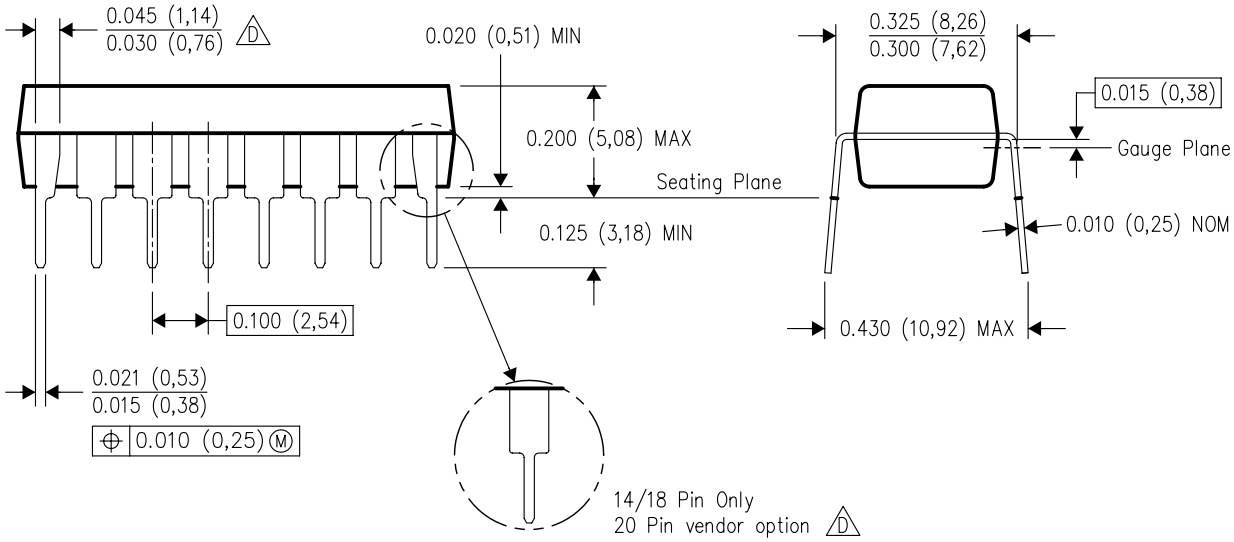
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



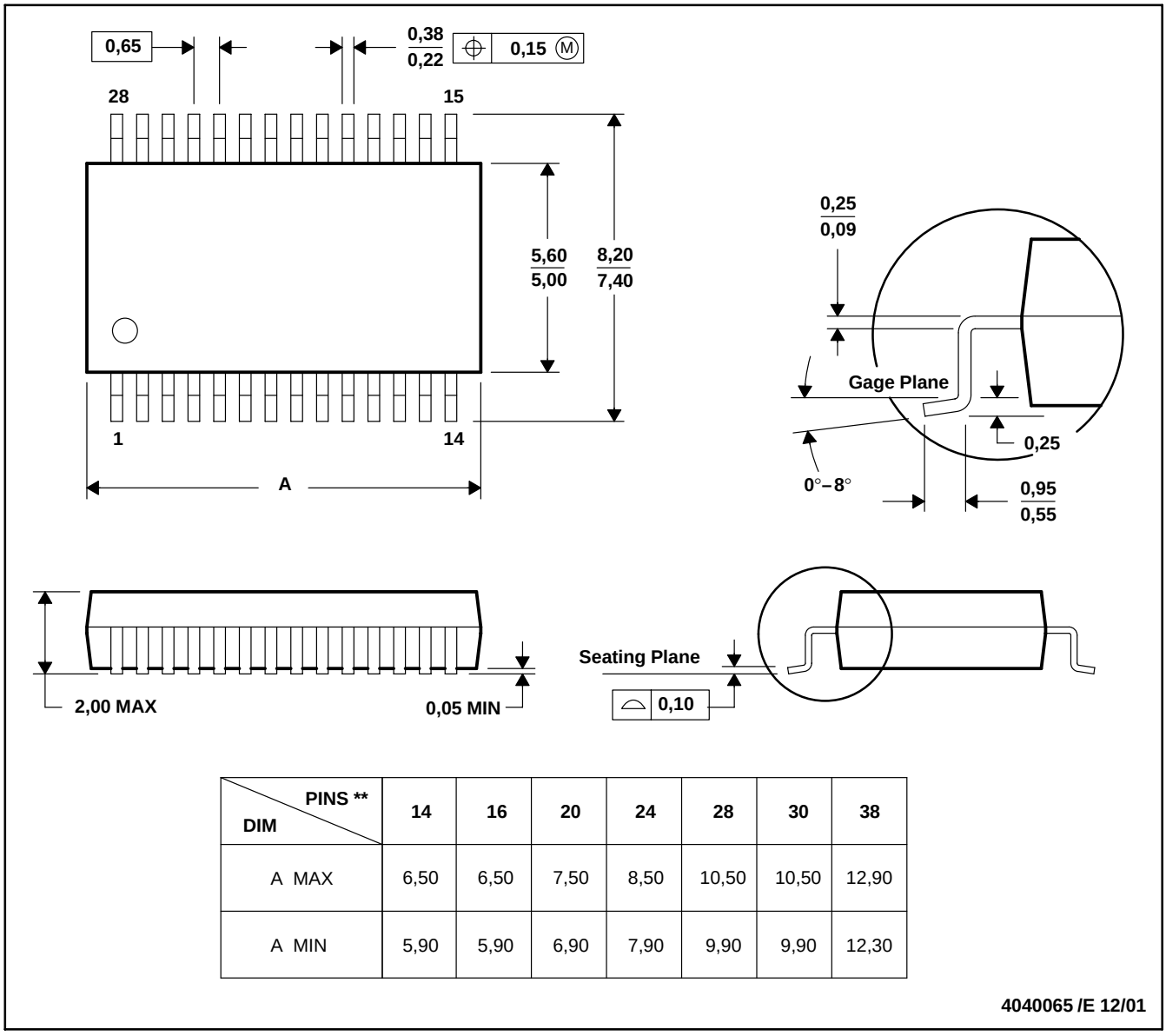
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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