TINSHARP Industrial Co., Ltd.

DATA SHEET

ISO 9001:2000 SGS SYSTEM CERTIFICATION

LCM MODULE

TG320240D-06T

Specification for Approval

APPROVED BY	CHECKED BY	PREPARED BY

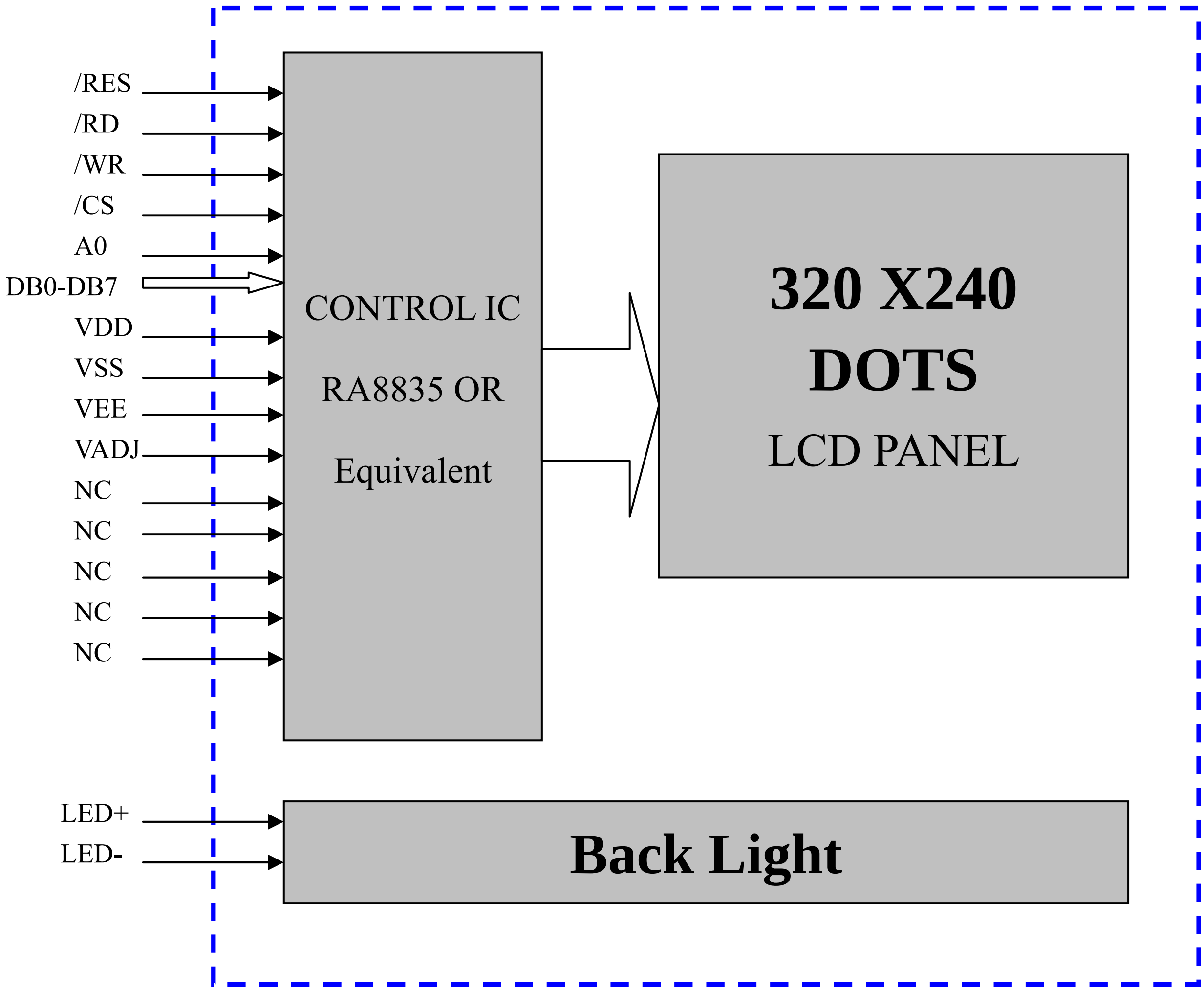
ISSUED: V00 2013-09-06

CONTENTS

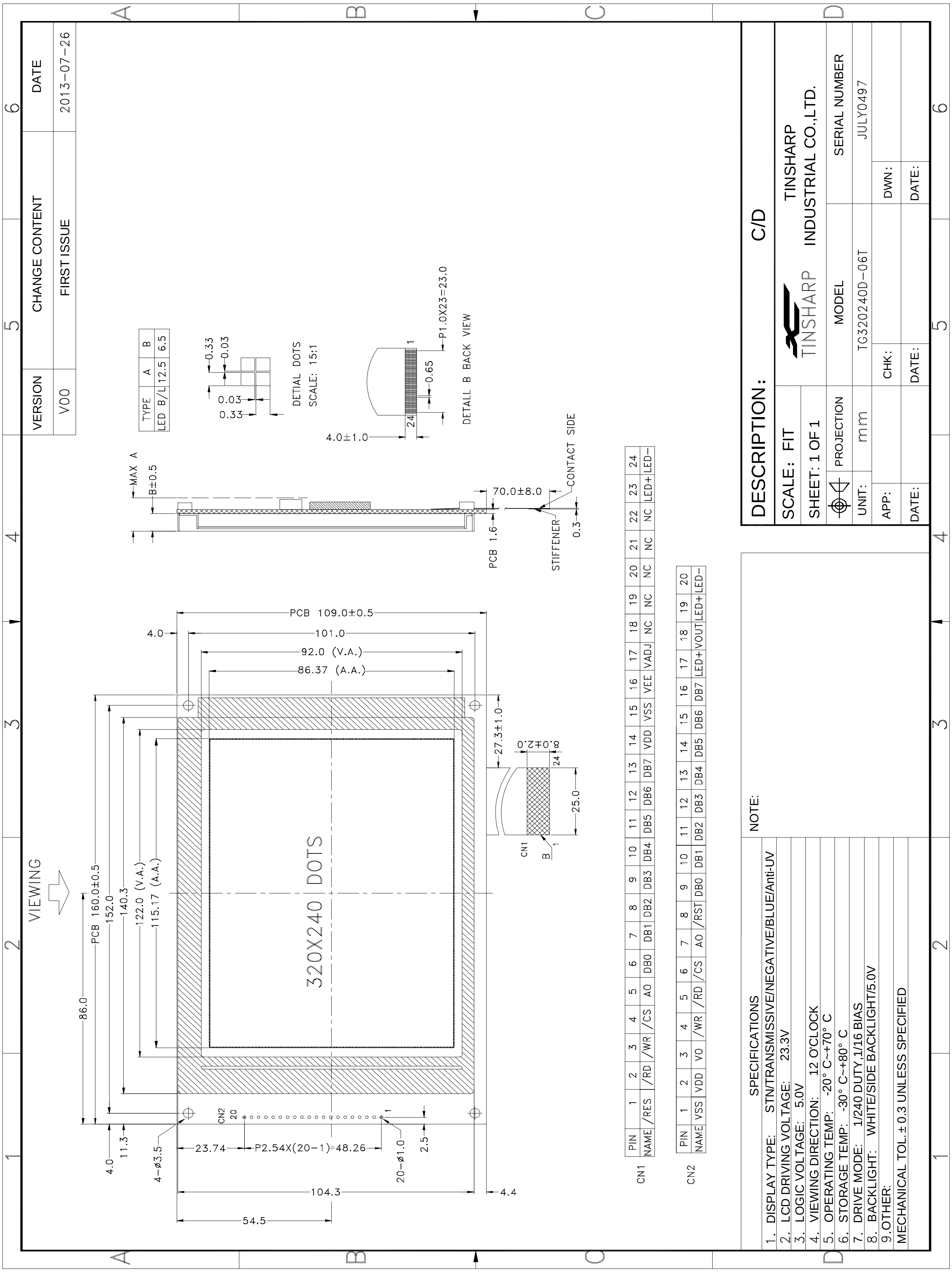
FUNCTIONS & FEATURES

- Construction : TAB
- Display Format : 320x240 dots
- Display Type : STN, Transmissive, Negative, Blue
- Controller : RA8835 or equivalent controller
- Interface : 8-bit parallel interface
- Backlight : white/ side Lights
- Viewing Direction :12 O'clock
- Driving Scheme : 1/240 Duty Cycle, 1/17 Bias
- Power Supply Voltage : 5.0 V
- V_{LCD} Adjustable For Best Contrast : 23.3 V (V_{OP}.)
- Operation temperature : -20℃ to +70℃
- Storage temperature : -30℃ to +80℃

BLOCK DIAGRAM



MODULE OUTLINE DRAWING



INTERFACE PIN FUNCTIONS

CN1:

Pin No.	Symbol	Level	Description
1	/RES	H/L	Reset signal, low level is active.
2	/RD	H/L	Read enable signal.
3	/WR	H/L	Write enable signal.
4	/CS	H/L	Chip selection is enable only when /CS is “L”.
5	A0	H/L	A0 = “H”: Indicates that DB0 to DB7 are control data. A0 = “L”: Indicates that DB0 to DB7 are display data.
6	DB0	H/L	8-bit bi-directional data bus.
7	DB1	H/L	
8	DB2	H/L	
9	DB3	H/L	
10	DB4	H/L	
11	DB5	H/L	
12	DB6	H/L	
13	DB7	H/L	
14	VDD	+5.0V	Supply voltage for logic operating.
15	VSS	0V	Ground.
16	VEE	--	Negative voltage supply for LCD
17	VADJ	--	Adjusting voltage of LCD contrast
18	NC	--	Non-connection
19	NC	--	Non-connection
20	NC	--	Non-connection
21	NC	--	Non-connection
22	NC	--	Non-connection
23	LED+	+5.0V	Power supply for Back Light.
24	LED-	0V	Ground for Back Light.

CN2:

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground.
2	VDD	+5.0V	Supply voltage for logic operating.
3	V0	--	Adjusting voltage of LCD contrast.
4	/WR	H/L	Write enable signal.
5	/RD	H/L	Read enable signal.
6	/CS	H/L	Chip selection is enable only when /CS is “L”.
7	A0	H/L	A0 = “H”: Indicates that DB0 to DB7 are control data. A0 = “L”: Indicates that DB0 to DB7 are display data.
8	/RST	H/L	Reset signal, low level is active.
9	DB0	H/L	8-bit bi-directional data bus.
10	DB1	H/L	
11	DB2	H/L	
12	DB3	H/L	
13	DB4	H/L	
14	DB5	H/L	
15	DB6	H/L	
16	DB7	H/L	
17	LED+	+5.0V	Power supply for Back Light.
18	VOUT	--	Negative voltage supply for LCD
19	LED+	+5.0V	Power supply for Back Light.
20	LED-	0V	Ground for Back Light.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	V_{DD}	-0.3	+7.0	V
Supply voltage for LCD	V_o	-0.3	+25	V
Input voltage	V_I	-0.3	V_{DD} +0.3	V
Normal Operating temperature	T_{OP}	-20	+70	℃
Normal Storage temperature	T_{ST}	-30	+80	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

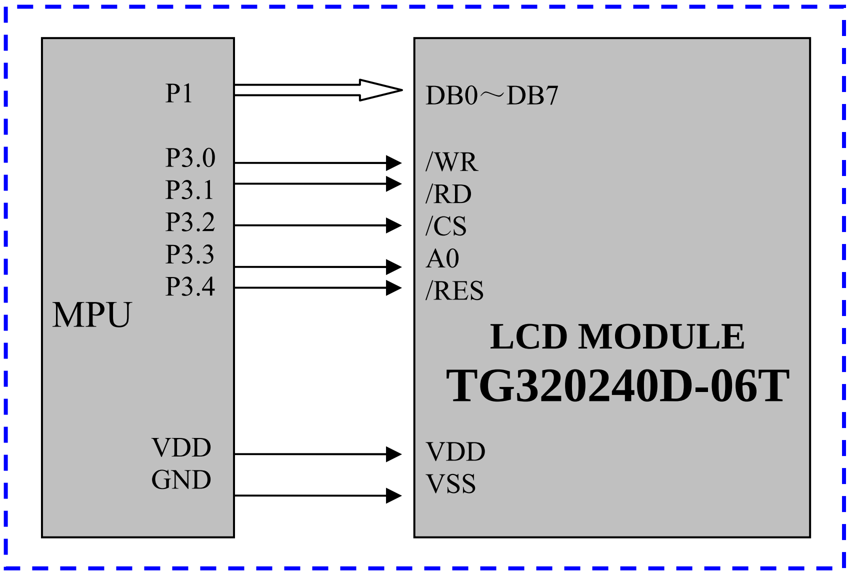
Parameter	Symbol	Condition	Min	T_{YP}	Max	Unit
Supply voltage for logic	VDD	--	4.8	5.0	5.2	V
Supply current for logic	IDD	--	--	160	180	mA
Operating voltage for LCD	VLCD	-20℃				
		+25℃	23.0	23.3	23.6	V
		+70℃				
Input voltage “H” level	VIH	--	0.5VDD	--	VDD	V
Input voltage “L” level	VIL	--	0	--	0.2VDD	V

LED BACKLIGHT CHARACTERISTICS

COLOR	Wavelength λ p(nm)	Operating Voltage(±0.15V)	Spectral line half width Δλ (nm)	Forward Current (mA)
white	--	3.0	--	130.0

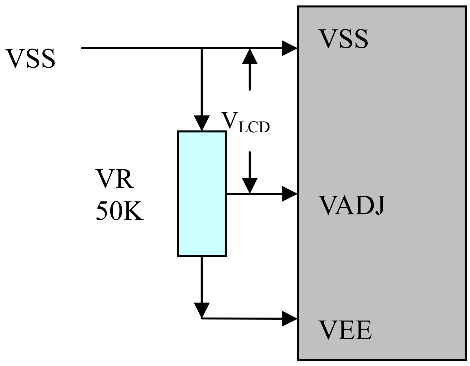
NOTE: Do not connect +5V directly to the backlight terminals. This will ruin the backlight.

CONNECTION WITH MCU



Typical V0 connections for display contrast

Adjust V0 to VDD (VLCD=+23.0V) as an initial setting. When the module is operational, readjust V0 for optimal display appearance.



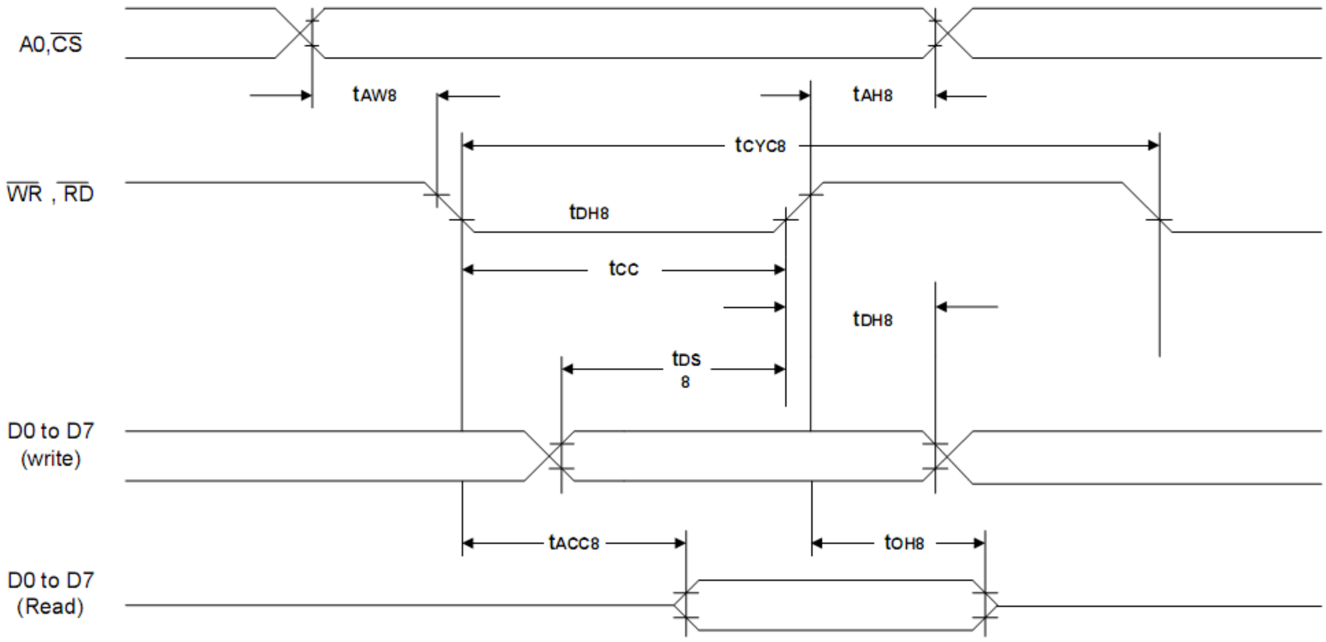
We recommend allowing field adjustment of V0 for all designs. The optimal value for V0 will change with temperature, variations in VDD, and viewing angle. V0 will also vary module-to-module and batch-to-batch due to normal manufacturing variations.

Ideally, adjustment to V0 should be available to the end user so each user can adjust the display to the optimal contrast for their required viewing conditions. As a minimum, your design should allow V0 to be adjusted as part of your product's final test.

Although a potentiometer is shown as a typical connection, V0 can be driven by your microcontroller, either by using a DAC or a filtered PWM. Displays that require V0 to be negative may need a level-shifting circuit. Please do not hesitate to contact Tinsharp application support for design assistance on your application.

AC CHARACTERISTICS

8080 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC8}	System cycle time	note.	—	note.	—	ns	
	t_{CC}	Strobe pulse width	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

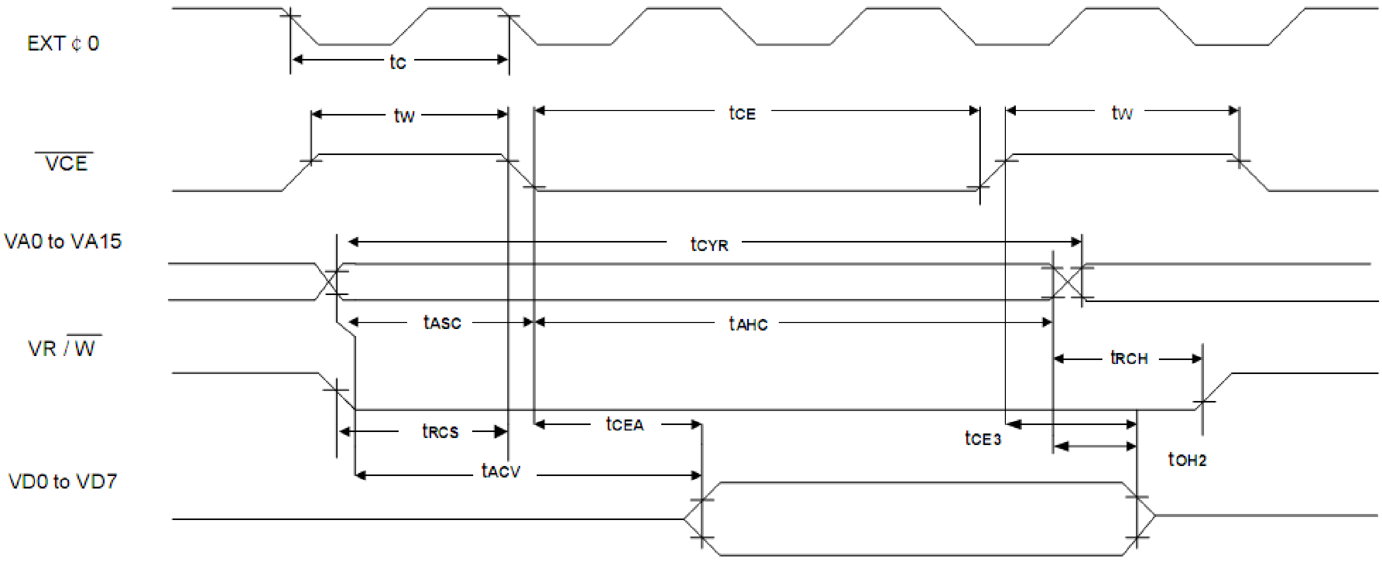
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

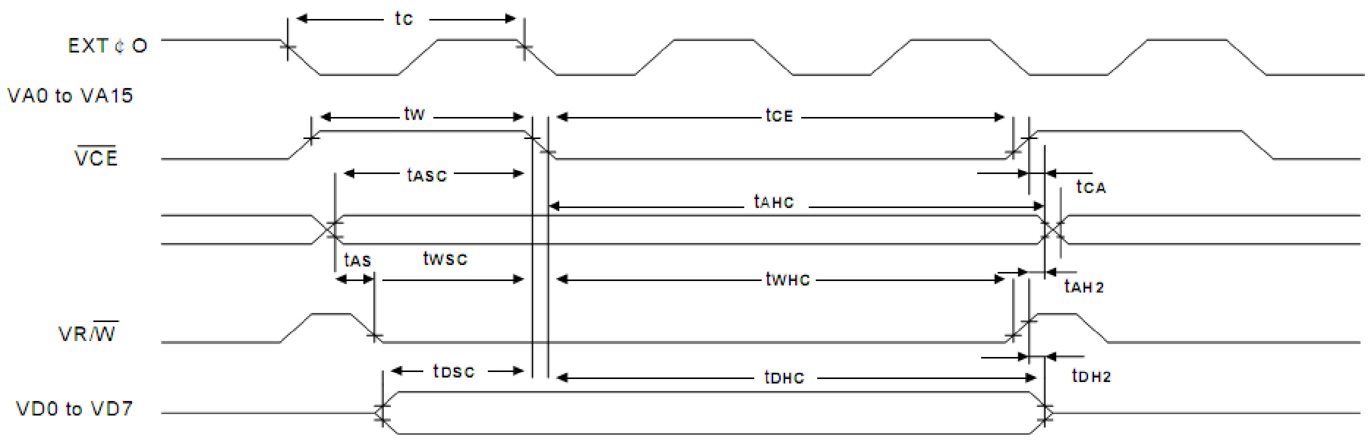
Display Memory Read Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{\text{VCE}}$	t_W	$\overline{\text{VCE}}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{\text{VCE}}$ LOW-level pulse width	$2t_C$ – 30	—	2 t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	$3t_C$	—	$3t_C$	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{\text{VCE}}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{\text{VCE}}$	2 t_C – 30	—	$2t_C$ – 40	—	ns	
$\overline{\text{VRD}}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{\text{VCE}}$	t_C – 45	—	t_C – 60	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{\text{VCE}}$	$0.5t_C$	—	$0.5t_C$	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	$3t_C$ – 100	—	$3t_C$ – 115	Ns	
	t_{CEA}	$\overline{\text{VCE}}$ access time	—	$2t_C$ – 80	—	$2t_C$ – 90	Ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{\text{VCE}}$ to data off time	0	—	0	—	ns	

Display Memory Write Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	$t_C - 50$	—	$t_C - 50$	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	$2t_C - 30$	—	$2t_C - 30$	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3tC	—	$3t_C$	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	$2t_C - 30$	—	$2t_C - 40$	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	$t_C - 70$	—	$t_C - 110$	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	$t_C - 80$	—	$t_C - 115$	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	$2t_C - 20$	—	$2t_C - 20$	—	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	$t_C - 85$	—	$t_C - 125$	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	$2t_C - 30$	—	$2t_C - 30$	—	ns	

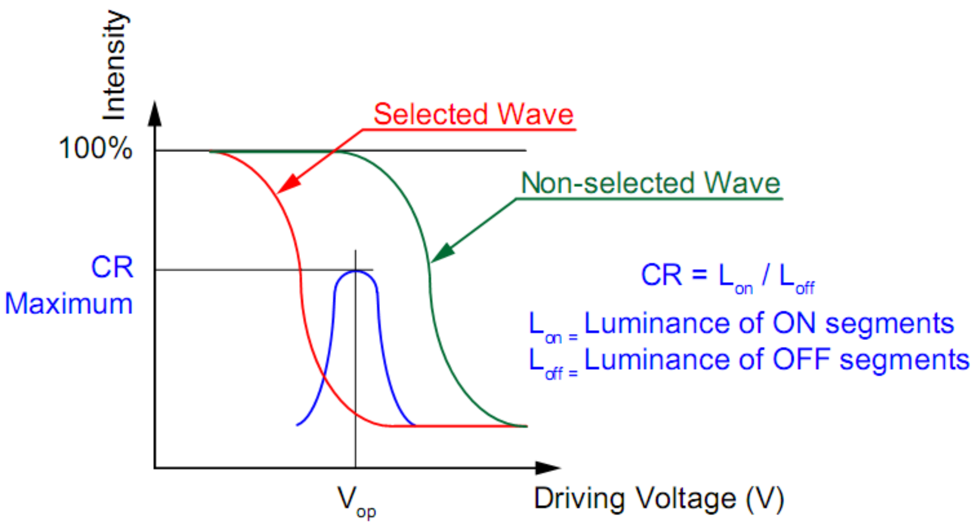
	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

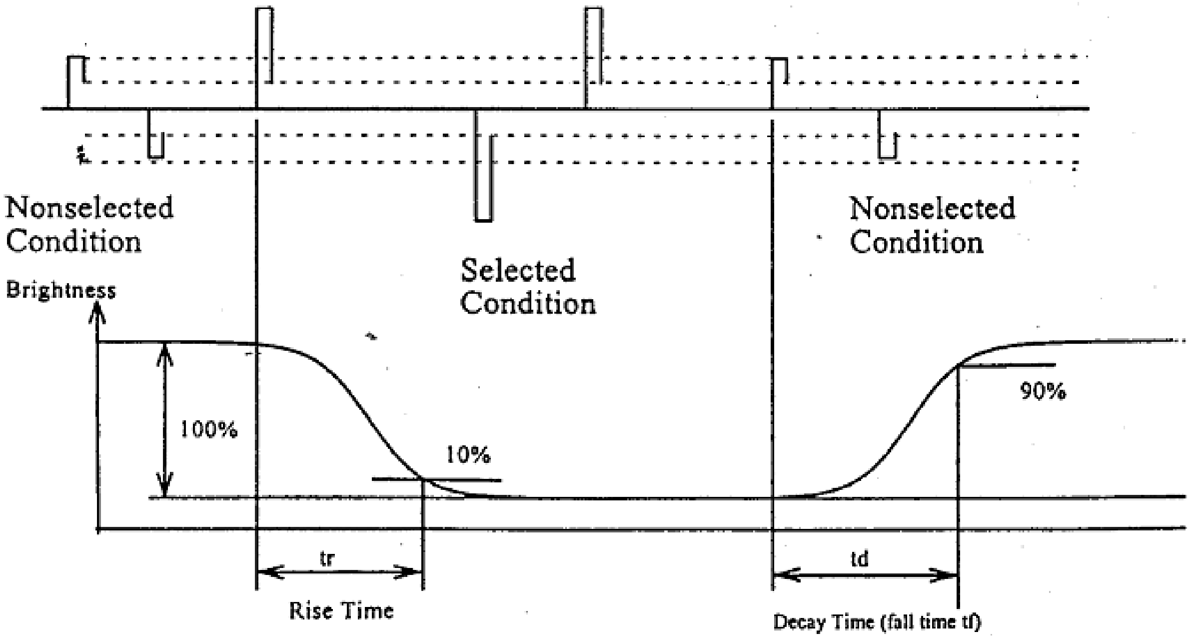
OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Contrast ratio	CR	θ=0，Φ=0	-	3	-		
Response time(rise)	Tr	25℃		-	250	ms	
Response time(fall)	Td			-	350		
Viewing angle	θf	25℃					
	θb						
	θl			-		deg.	
	θr			-			

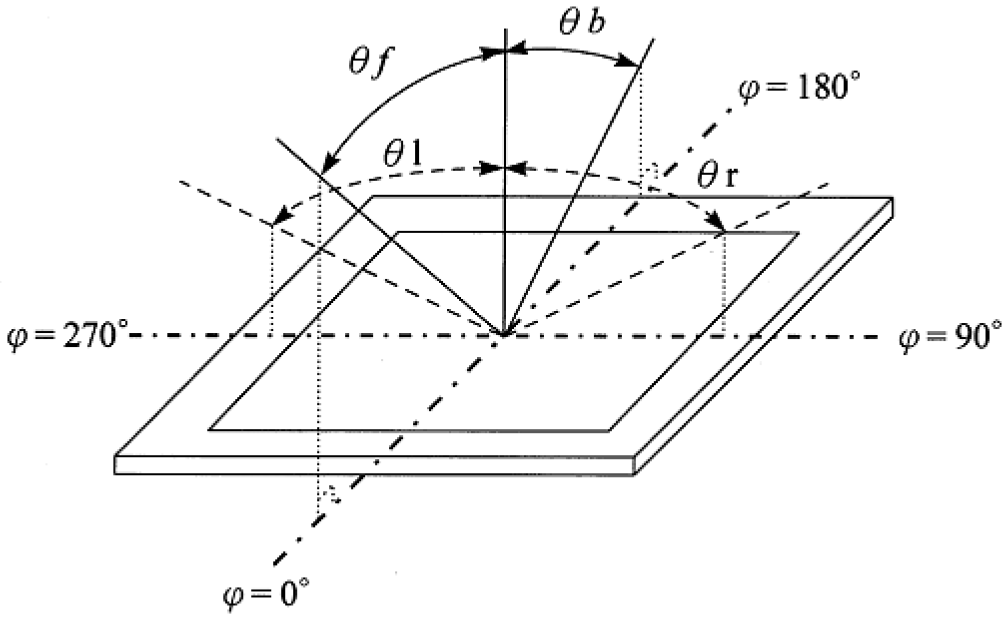
Note1: Definition Operation Voltage (Vop.)



Note2: Response time



Note3: Viewing angle



COMMAND SET

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	9-2-1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	9-2-2
Display Control	DISPLAY ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	9-3-1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	9-3-2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	9-3-3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	9-3-6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	9-3-4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	9-3-7

	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	9-3-5
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	9-r1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	9-4-2
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	9-5-1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	9-5-2

Notes:

1. In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

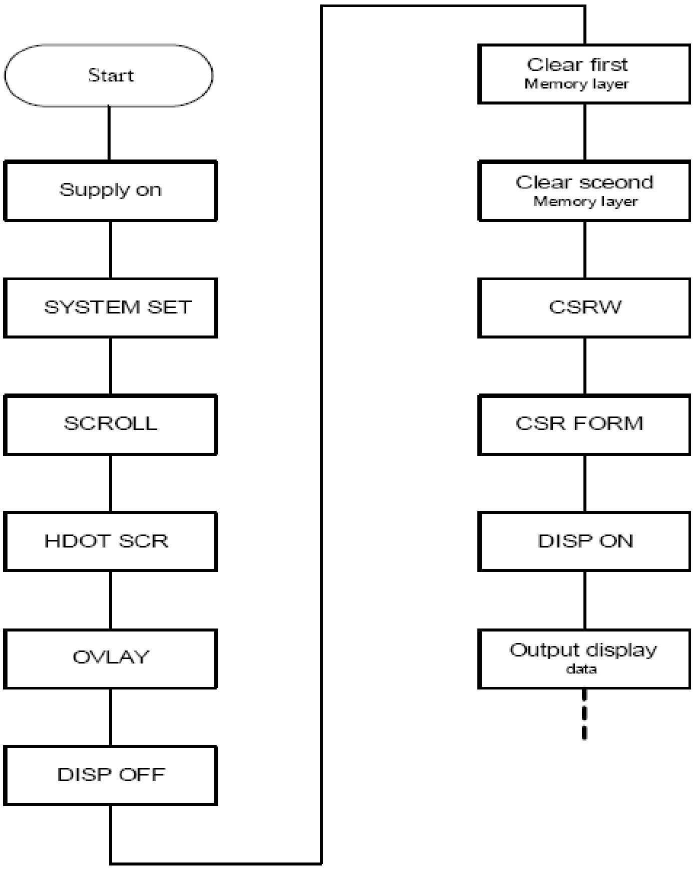
    a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

    b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

INITIALIZATION EXAMPLE

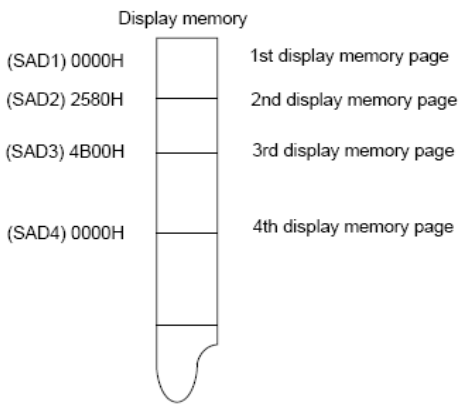
The initialization example shown in Figure 8-1 is for a RA8835 series with an 8-bit microprocessor interface bus and a display unit (320 x 240 pixels).



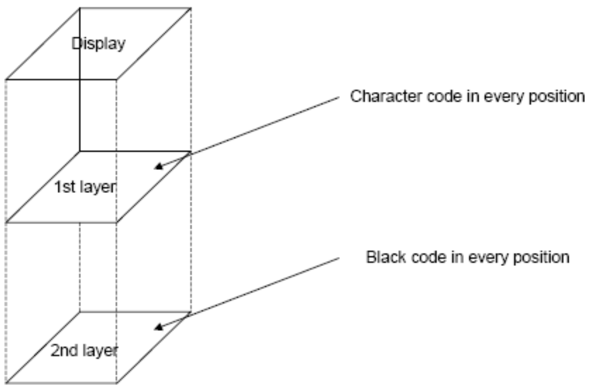
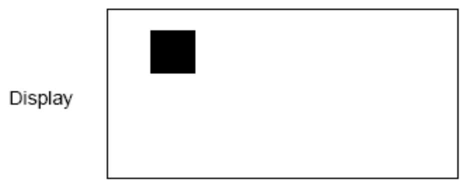
Note: Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20H (text screen only) or 00H (graphics screen only). Determining which memory to clear is explained in section 17-1-3.

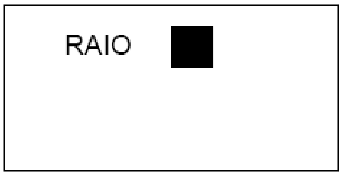
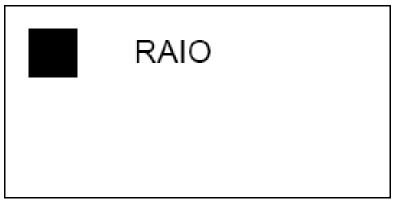
INITIALIZATION PROCEDURE

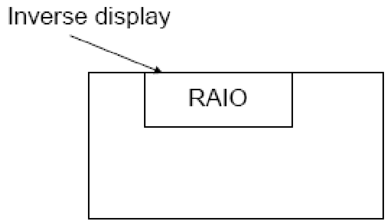
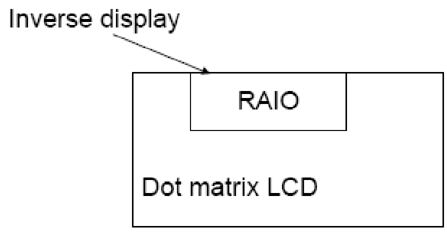
No.	Command	Operation
1	Power-up	
2	Supply	
3	SYSTEM SET	
	C = 40H	
	P1 = 30H	M0: Internal CG ROM M1: CG RAM is 32 characters maximum M2: 8 lines per character W/S: Two-panel drive IV: No top-line compensation
	P2 = 87H	FX: Horizontal character size = 8 pixels WF: Two-frame AC drive
	P3 = 07H	FY: Vertical character size = 8 pixels
	P4 = 27H	C/R: 39 display addresses per line
	P5 = 2FH	TC/R: Total address range per line = 47 f_{OSC} = 8.0 MHz, f_{FR} = 70 Hz
	P6 = EFH	L/F: 239 display lines
	P7 = 28H	AP: Virtual screen horizontal size is 40 addresses
	P8 = 00H	
4	SCROLL	
	C = 44H	
	P1 = 00H	First screen block start address
	P2 = 00H	Set to 0000H
	P3 = F0H	Display lines in first screen block = 240
	P4 = 80H	Second screen block start address
	P5 = 25H	Set to 1000H
	P6 = F0H	Display lines in second screen block = 240
	P7 = 00H	Third screen block start address
	P8 = 4BH	Set to 4B00H
	P9 = 00H	Fourth screen block start address
	P10 = 00H	Set to 0000H



No.	Command	Operation
5	HDOT SCR	
	C = 5AH	
	P1 = 00H	Set horizontal pixel shift to zero

No.	Command	Operation
6	OVLAY C = 5BH P1 = 01H	MX 1, MX 0: Inverse video superposition DM 1: First screen block is text mode DM 2: Third screen block is text mode
7	DISP ON/OFF C = 58H P1 = 56H	D: Display OFF FC1, FC0: Flash cursor at 2 Hz FP1, FP0: First screen block ON FP3, FP2: Second and fourth screen blocks ON FP5, FP4: Third screen block ON
8	Clear data in first layer	Fill first screen layer memory with 20H (space character)
9	Clear data in second layer	Fill second screen layer memory with 00H (blank data) 
10	CSRW C = 46H P1 = 00H P2 = 00H	Set cursor to start of first screen block
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	CRX: Horizontal cursor size = 5 pixels CRY: Vertical cursor size = 7 pixels CM: Block cursor
12	DISP ON/OFF C = 59H	Display ON 
13	CSR DIR C = 4CH	Set cursor shift direction to right

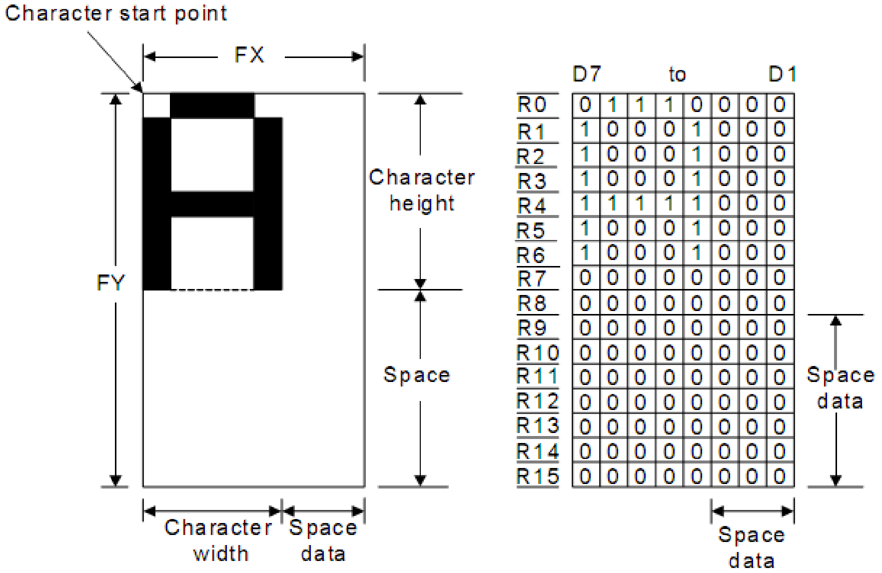
No.	Command	Operation
14	MWRITE	
	C = 42H	
	P1 = 20H	‘ ’
	P2 = 52H	‘R’
	P3 = 41H	‘A’
	P4 = 49H	‘I’
	P5 = 4FH	‘O’
		
15	CSRW	
	C = 46H	
	P1 = 00H	Set cursor to start of second screen block
	P2 = 10H	
16	CSR DIR	
	C = 4FH	Set cursor shift direction to down
17	MWRITE	
	C = 42H	
	P1 = FFH	Fill a square to the left of the ‘E’
	↓	
	P9 = FFH	
		
18	CSRW	
	C = 46H	
	P1 = 01H	Set cursor address to 1001H
	P2 = 10H	
19	MWRITE	
	C = 42H	
	P1 = FFH	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFH	

No.	Command	Operation
20	CSRW	Repeat operations 18 and 19 to fill in the background under ‘RAIO’
↓		
29	MWRITE	
30	CSRW C = 46H P1 = 00H P2 = 01H	Set cursor to line three of the first screen block
31	CSR DIR C = 4CH	Set cursor shift direction to right
32	MWRITE C = 42H	
	P1 = 44H ‘D’	
	P2 = 6FH ‘o’	
	P3 = 74H ‘t’	
	P4 = 20H ‘ ’	
	P5 = 4DH ‘M’	
	P6 = 61H ‘a’	
	P7 = 74H ‘t’	
	P8 = 72H ‘r’	
	P9 = 69H ‘i’	
	P10 = 78H ‘x’	
	P11 = 20H ‘ ’	
	P12 = 4CH ‘L’	
	P13 = 43H ‘C’	
	P14 = 44H ‘D’	

CHARACTER

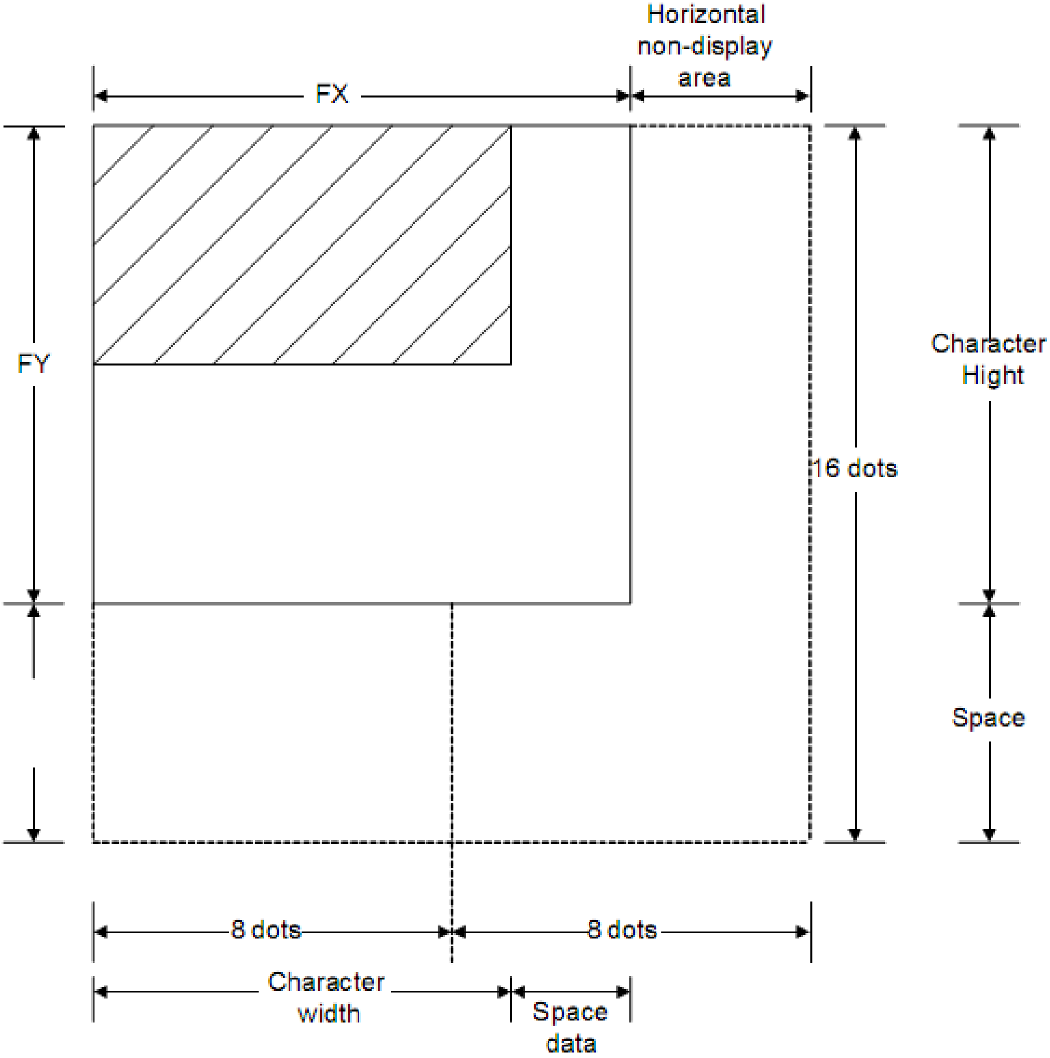
CHARACTER CONFIGURATION:

The origin of each character bitmap is in the top left corner as shown in Figure 7-9. Adjacent bits in each byte are horizontally adjacent in the corresponding character image. Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.



Example of Character Display ([FX] ≤ 8) and Generator Bitmap

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank. The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.



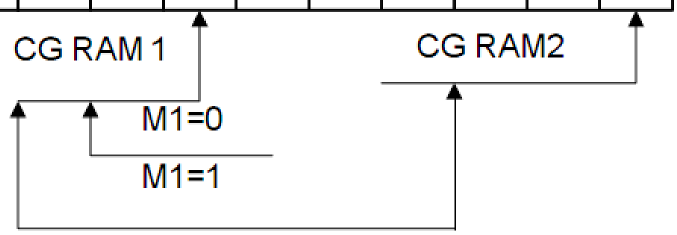
Character Width Greater Than One Byte Wide ([FX]=9)

Note: The RA8835 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

CHARACTER CODES

The following figure shows the character codes and the codes allocated to CG RAM. The CG RAM if not using the internal ROM can use all codes.

	Upper 4bites															
Lower 4bites	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				0	@	P	‘	p								
1			!	1	A	Q	a	q								
2			“	2	B	R	b	r								
3			#	3	C	S	c	s								
4			$	4	D	T	d	t								
5			&	5	E	U	e	u								
6			%	6	F	V	f	v								
7			'	7	G	W	g	w								
8			(	8	H	X	h	x								
9			)	9	I	Y	i	y								
A			*	:	J	Z	j	z								
B			+	;	K	[	k	{								
C			,	<	L	¥	l	¦								
D			.	=	M	]	m	}								
E			-	>	N	^	n	→								
F			/	?	O	_	o	←								



RELIABILITY TEST CONDITION

No.	TEST Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80° C 96hrs	------
2	Low temperature storage	Endurance test applying the low storage Temperature for a long time	-30° C 96hrs	-----
3	High temperature operation	Endurance test applying the electric stress (Voltage & current)and the thermal stress to the element for a long time	70° C 96hrs	------
4	Low temperature operation	Endurance test applying the electric stress Under low temperature for a long time	-20° C 96hrs	------
5	High temperature/ Humidity storage	Endurance test applying the electric stress(Voltage & current) and Temperature/ Humidity stress to the element for a long time	40° C 90%RH 96hrs	
6	High temperature/ Humidity operation	Endurance test applying the electric stress (voltage & current)and temperature/ humidity stress to the element for a long time	40° C 90%RH 96hrs	
7	Temperature cycle	Endurance test applying the low and high temperature cycle. -20° C →25° C→70° C 30min←5min←30min.(1 cycle)	-20° C/70° C 10 cycle	------

Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25° C.

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	

Environmental condition

The inspection should be performed at the 1metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

PRECAUTION FOR USING LCM MODULE

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
  Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0℃).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections

A. DATE CODE RULES

A.1. DATE CODE FOR SAMPLE

YP: meaning sample

TG320240D-06T	→ LCM part number
YP XXXXX	→ Sample array No.

A.2. DATE CODE FOR PRODUCTION

TG320240D-06T	→ LCM part number
YY/WW/XXXXXXXX	→ Production date and Production array

A. TG320240D-06T represents LCM part number

C. YY/WW represents Year, Week

YY—Year WW—Week

XXXXXXXX—Production array No.

B. CHANGE NOTES:

Ver.	Descriptions	Editor	Date
V00	First Issue	ZXQ	2013-09-06