FORMIKE ELECTRONIC CO.,LTD

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH040ST03-F02 Version: 1.0

【 ◆ 】 Preliminary Specification

【 】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATA:

Designed by	R&D Checked by	Quality Department by	Approved by
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● This specification is subject to change without notice. Please contact FORMIKE or it's representative before designing your product based on this specification.

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1. Revision record

VEV NO.	REV DATE	CONTENTS	Note
V1.0	**2013-12-18**	**NEW ISSUE**	

2. General Description

2.1 Description

KWH040ST03-F02 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC,TP and backlight unit . The following table described the features of FORMIKE KWH040ST03-F02.

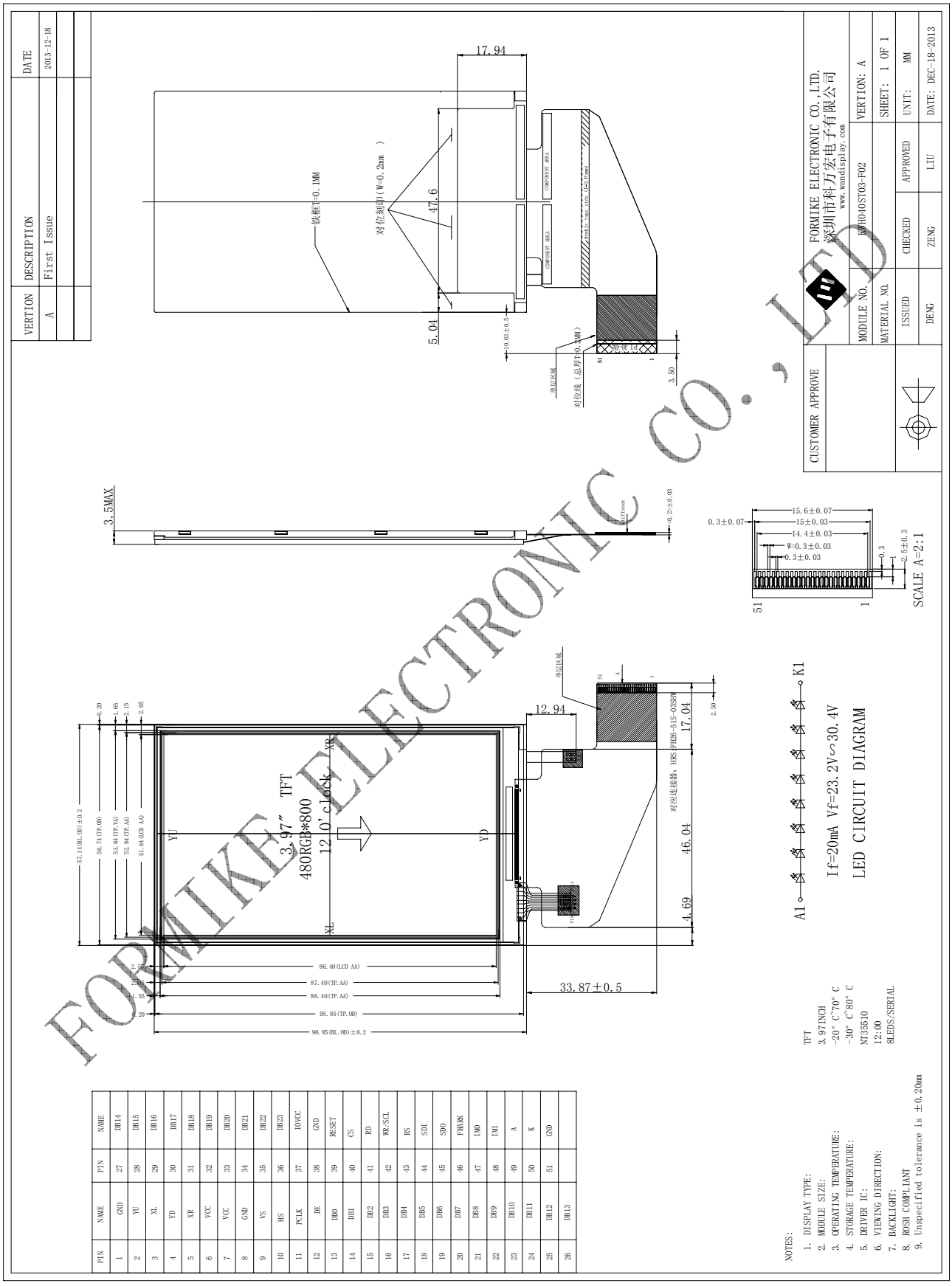
2.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

2.3 Features:

Features	Description	UNITS
LCD type	3.97”TFT	--
Dot arrangement	480（RGB）×800	dots
Driver IC	NT35510	--
Color Depth	16.7M	
Interface	RGB ,MCU Interface	--
View Direction	12 O’clock	--
Module size	57.14(W) ×96.85 (H)×3.50(T)	mm
Active area	51.84(W) ×86.4(H)	mm
Dot pitch	0.108 (W) ×0.108 (H)	mm
Back Light	8 White LED In serial	--
With/Without TSP	With TSP	
Weight(g)	TBD	

3. External Dimensions



PIN	NAME	PIN	NAME
1	GND	27	DB14
2	YU	28	DB15
3	XL	29	DB16
4	YD	30	DB17
5	XR	31	DB18
6	VCC	32	DB19
7	VCC	33	DB20
8	GND	34	DB21
9	VS	35	DB22
10	HS	36	DB23
11	PCLK	37	IOVCC
12	DE	38	GND
13	DB0	39	RESET
14	DB1	40	CS
15	DB2	41	RD
16	DB3	42	WR/SCL
17	DB4	43	RS
18	DB5	44	SDI
19	DB6	45	SDO
20	DB7	46	FMARK
21	DB8	47	LMD
22	DB9	48	LM1
23	DB10	49	A
24	DB11	50	K
25	DB12	51	GND
26	DB13		

NOTES:
1. DISPLAY TYPE: TFT
2. MODULE SIZE: 3.97INCH
3. OPERATING TEMPERATURE: -20° C~70° C
4. STORAGE TEMPERATURE: -30° C~80° C
5. DRIVER IC: NT35510
6. VIEWING DIRECTION: 12:00
7. BACKLIGHT: 8LEDS/SERIAL
8. ROSH COMPLIANT
9. Unspecified tolerance is ±0.20mm

4. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground.
2	YU	Touch Panel Up Side Wire.
3	XL	Touch Panel Left Side Wire.
4	YD	Touch Panel Down Side Wire.
5	XR	Touch Panel Right Side Wire.
6-7	VCC	Power supply (+2.3V~+4.8V).
8	GND	Ground.
9	VS	Frame synchronizing signal for RGB interface operation. Fix to GND level when not in use.
10	HS	Line synchronizing signal for RGB interface operation. Fix to GND level when not in use.
11	PCLK	Dot clock signal for RGB interface operation. Fix to GND level when not in use.
12	DE	Data enable signal for RGB interface operation. Fix to GND level when not in use.
13-36	DB0-DB23	24-Bit parallel data bus for 8080 system and RGB interface mode. Fix to GND level when not in use.
37	IOVCC	Power supply Voltage for I/O Interface (+1.65V~+3.3V).
38	GND	Ground.
39	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
40	CS	Chip select input pin(“ low” enable).
41	RD	8080 system(RD):Serves as a read signal and MCU read data at the rising edge. Fix to GND when not in use.
42	WR/SCL	8080 system(WR):Serves as a write signal and writes data at the rising edge. SCL: a synchronous clock in SPI Interface. Fix to GND level when not in use.
43	RS	This pin is used to select ”data or command” in the 8080 system interface When RS=”1”, data is selected. When RS=”0”, command is selected. Fix to GND when not in use.
44	SDI	Serial input signal in SPI interface. The data is input on the rising edge of the SCL signal. Fix to GND when not in use.
45	SDO	Serial output signal in SPI interface. The data is output on the rising edge of the SCL signal. Fix to open when not in use.
46	FMARK	Tearing effect output pin to Synchronous MCU to frame writing. activated by S/W command. If not used, please open this pin.
47	IM0	Interface type selection:
48	IM1	IM1 IM0 SRAM Register 0 0 80-8bit MPU I/F80-8bit MPU I/F DB[7:0]

		0	1	80-16bit MPU	I/F80-8bit MPU I/F DB[15:0]
		1	0	80-24bit MPU	I/F80-8bit MPU I/F DB[23:0]
		1	1	24bit RGB	RGB I/F DB[23:0]
49	A	Power supply for LED backlight Anode input.			
50	K	Power supply for LED backlight Cathode input.			
51	GND	Ground.			

5. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VDDA, VDDB, VDDR,VDDAM	-0.3 ~ +5.5	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +5.5	V
Supply voltage (Digital)	DVDD,DIOPWR	-0.3 ~ +2.0	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ +6.6	V
	AVEE-AVSS	+0.3 ~ -6.6	V
Supply voltage (HV)	VGH-VGLX (VGHO-VGLO)	-0.3 ~ +33	V
Logic Input voltage range	VIN	- 0.3 ~ VDDI + 0.3	V
Logic Output voltage range	VO	- 0.3 ~ VDDI + 0.3	V
Differential Input Voltage	HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N	-0.3 ~ +1.8	V
Operating temperature range	TOPR	-40 ~ +85	ºC
Storage Temperature range	TSTG	-55 ~ +125	ºC

NOTE:

If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6. Electrical Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.3	3.7	4.8	V	Note 1, 2
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1, 2
	VDDIL	I/O supply voltage	1.1	1.2	1.3	V	
Input / Output							
Logic High level input voltage	VIH	VDDI=1.65~3.3V	0.7 VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL	VDDI=1.65~3.3V	VSSI	-	0.3 VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	VDDI=1.65~3.3V IOH = -1.0mA	0.8 VDDI	-	VDDI	V	Note 1, 2, 5
Logic Low level output voltage	VOL	VDDI=1.65~3.3V IOL = +1.0mA	VSSI	-	0.2 VDDI	V	Note 1, 2, 5
Logic High level leakage (Except MIPI/MDDI)	ILIH	Vin=0~VDDI	-	-	1	μA	Note 1, 2, 3
Logic Low level leakage (Except MIPI/MDDI)	ILIL	Vin=0~VDDI	-1	-	-	μA	Note 1, 2, 3
Logic High level leakage (MIPI/MDDI)	ILIH	Vin=0~VDDAM	-	-	1	μA	Note 2, 8
Logic Low level leakage (MIPI/MDDI)	ILIL	Vin=0~VDDAM	-1	-	-	μA	Note 2, 8
DC/DC Converter Operation							
AVDD booster voltage	AVDD	-	4.5	-	6.5	V	Note 2, 7
AVEE booster voltage	AVEE	-	-6.5	-	-4.5	V	Note 2, 7
VCL booster voltage	VCL	-	-2.5	-	-4.0	V	Note 2, 7
VGH booster voltage	VGH	-	AVDD +VDDB	-	2AVDD -AVEE	V	Note 2, 6
VGLX booster voltage	VGLX	-	AVEE +VCL	-	2AVEE -AVDD	V	Note 2, 6
Voltage difference between VGH and VGLX	VGHL	|VGH-VGLX|	-	-	30	V	Note 2
Oscillator tolerance	ΔOSC	25 ºC	-5	-	5	%	
Source Driver							
Gamma reference voltage	VGMP	-	3.0	-	6.3	V	Note 2
	VGSP	-	0.0	-	3.7	V	Note 2
	VGMN	-	-6.3	-	-3.0	V	Note 2
	VGSN	-	-3.7	-	0.0	V	Note 2
Output offset voltage	VOFSET	-	-	-	45	mV	Note 4
Output deviation voltage	Vdev	Sout≥4.0V, Sout≥1.0V	-	-	20	mV	Note 4
		1.0V<Sout<4.0V	-	-	10	mV	Fig.7.5.2

7.Timing Characteristics.

7.1 Reset Timing Characteristics.

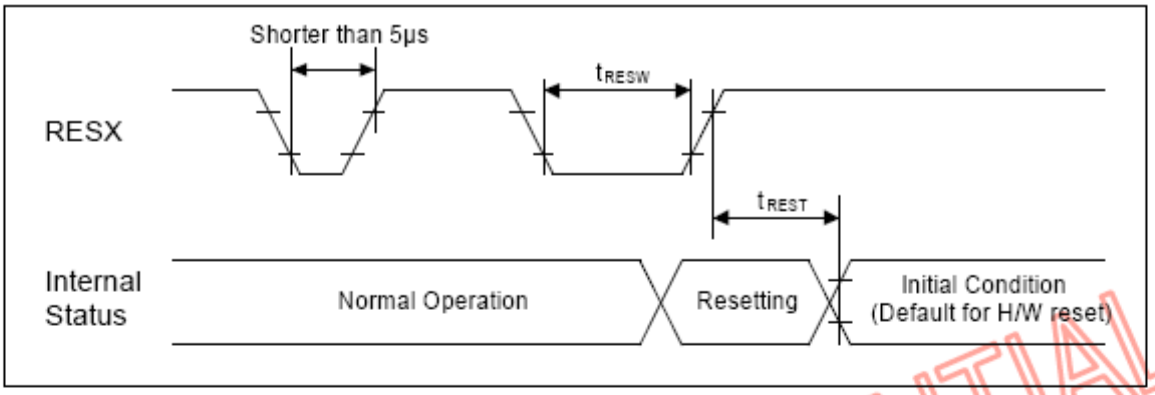


Fig. 7.6.12 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

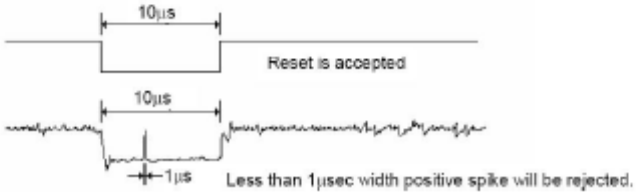
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7.2. i80-System Interface Timing Characteristics.

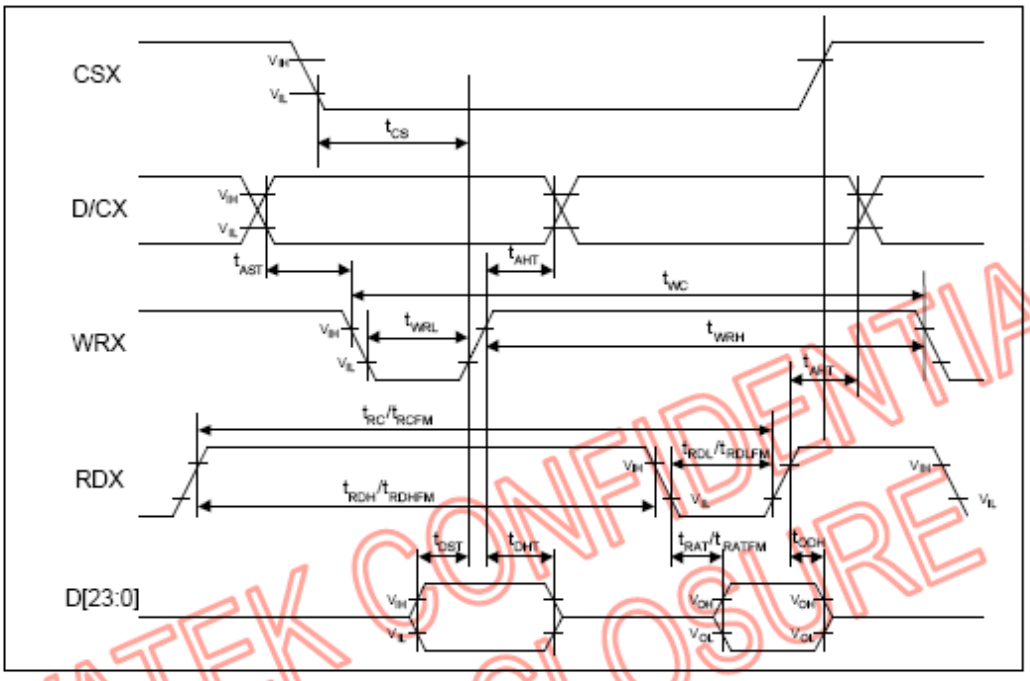


Fig. 7.6.1 Parallel interface characteristics (80-Series)

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
WRX	tWC	Write cycle	33	-	ns	
	tWRH	Control pulse "H" duration	15	-	ns	
	tWRL	Control pulse "L" duration	15	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90	-	ns	
	tRDL	Control pulse "L" duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	400	-	ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	250	-	ns	
	tRDLFM	Control pulse "L" duration (FM)	150	-	ns	
D/CX	tAST	Address setup time (Write)	0	-	ns	
		Address setup time (Read)	10	-	ns	
	tAHT	Address hole time	2	-	ns	
D[17:0]	tDST	Data setup time	15	-	ns	
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	150	ns	
	tODH	Output disable time	5	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.3. SPI Interface Timing Characteristics.

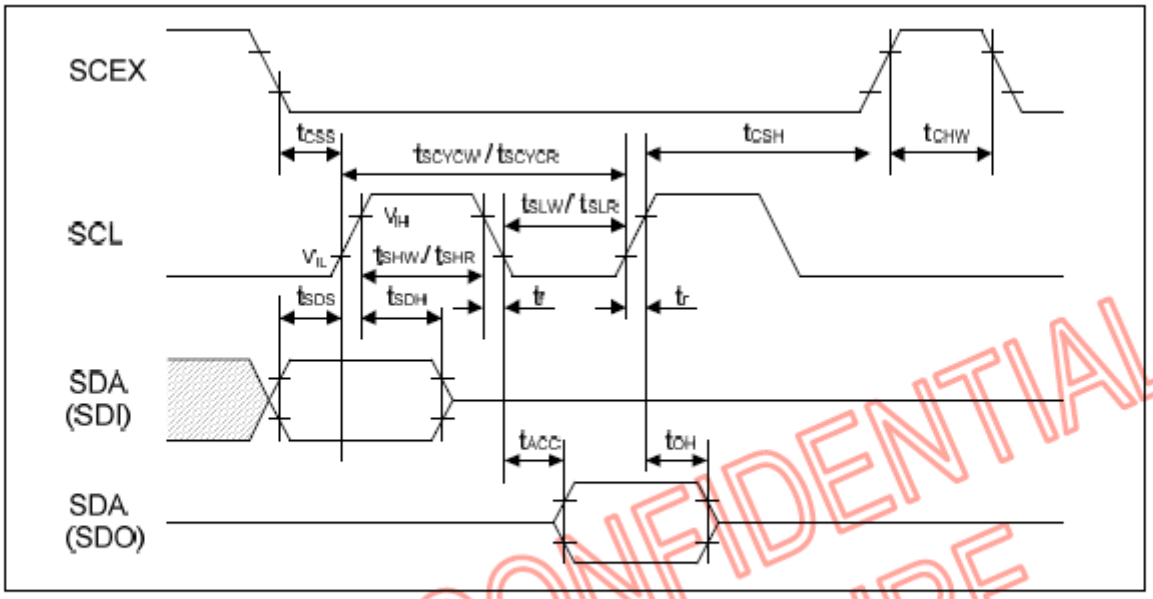


Fig. 7.6.2 3-pin serial interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	tSCYCW	Serial clock cycle (Write)	100	-	ns	
	tSHW	SCL "H" pulse width (Write)	40	-	ns	
	tSLW	SCL "L" pulse width (Write)	40	-	ns	
	tSCYCR	Serial clock cycle (Read GRAM)	300	-	ns	
	tSHR	SCL "H" pulse width (Read GRAM)	140	-	ns	
	tSLR	SCL "L" pulse width (Read GRAM)	140	-	ns	
	tSCYCR	Serial clock cycle (Read ID)	300	-	ns	
	tSHR	SCL "H" pulse width (Read ID)	140	-	ns	
	tSLR	SCL "L" pulse width (Read ID)	140	-	ns	
SDI (SDO)	tSDS	Data setup time	20	-	ns	
	tSDH	Data hold time	20	-	ns	
	tACC	Access time	-	120	ns	
	tOH	Output disable time	5	-	ns	
CSX	tCHW	Chip select "H" pulse width	45	-	ns	
	tCSS	Chip select setup time	20	-	ns	
	tCSH	Chip select hold time	50	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

7.4. RGB Interface Timing Characteristics.

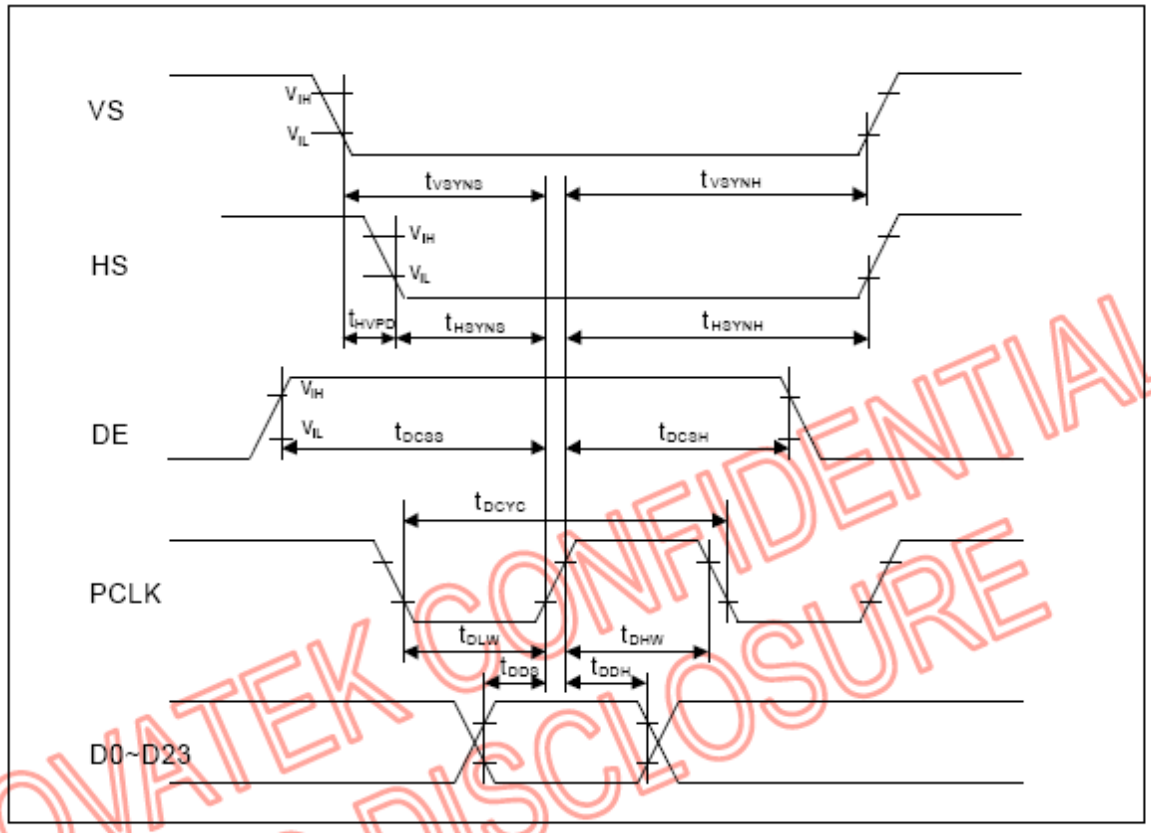


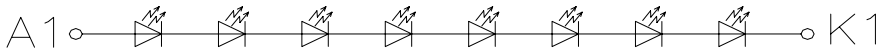
Fig. 7.6.4 RGB interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VS	tVSYNS	VSYNC setup time	10	-	-	ns	
	tVSYNH	VSYNC hold time	10	-	-	ns	
HS	tHSYNS	HSYNC setup time	10	-	-	ns	
	tSCYCR	HSYNC hold time	10	-	-	ns	
	tHVPD	HSYNC to VSYNC falling edge	400	-	-	ns	
PCLK	tDCYC	PCLK cycle time	33	-	125	ns	
	tDLW	PCLK "L" pulse width	11	-	-	ns	
	tDHW	PCLK "H" pulse width	11	-	-	ns	
	fDFREQ	PCLK frequency	8	-	30	MHz	
DE	tDCSS	DE setup time	10	-	-	ns	
	tDCSH	DE hold Time	10	-	-	ns	
D0~D23	tDDS	RGB Data setup time	10	-	-	ns	
	tDDH	RGB Data hold time	10	-	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

8. Backlight Characteristics.



If=20mA Vf=23.2V∽30.4V

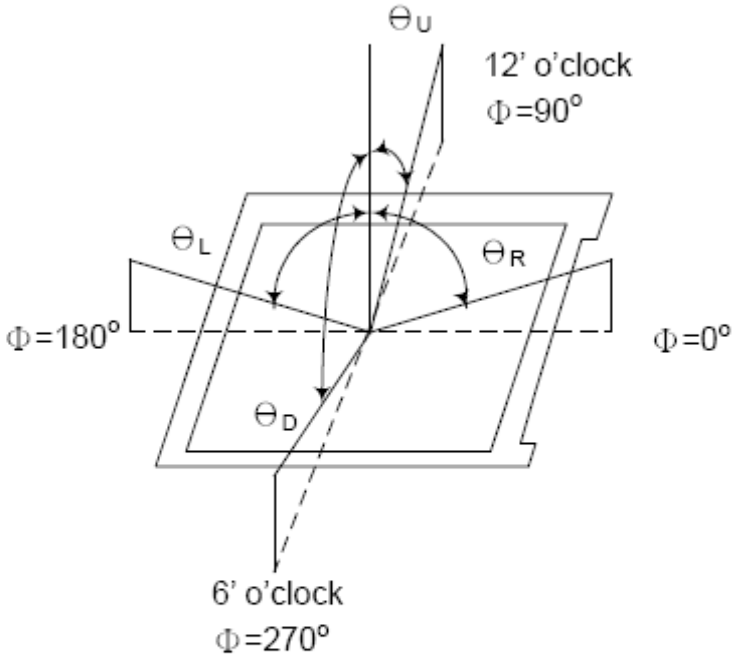
LED CIRCUIT DIAGRAM

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	**Vf**	**23.2**	**25**	**30.4**	**V**	**If=20 mA**	**-**
Supply Current	**If**	**-**	**20**	**-**	**mA**	**-**	**-**
Reverse Voltage	**Vr**	**-**	**-**	**5**	**V**	**10uA**	
Power dissipation	**Pd**	**-**	**500**	**-**	**mW**	**-**	
Luminous Intensity for LCM		-	**280**	-	**Cd/m²**	**If=20 mA**	
Uniformity for LCM	**-**	**80**	**-**	**-**	%	**If=20 mA**	
Life Time	**-**	**50000**	**-**	**-**	**Hr**	**If=20 mA**	**-**
Backlight Color	**White**						

9.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)		3.6	4.0	—	—	Transmittance base on using EWV Polarizer , Reference Only
Transmittance (without Polarizer)		T (%)		9.56	10.39	—	—	
Contrast		CR		560	700	—		(1)(2)
Response time	Rising	T_R	Θ=0 Normal viewing angle	—	4	8	msec	(1)(3)
	Falling	T_F		—	12	24		
Color gamut	S(%)			54	60	—	%	
Color chromaticity (CIE1931)	White	W_x		0.266	0.296	0.326		(1)(4) CF glass
		W_y		0.295	0.325	0.355		
	Red	R_x		0.617	0.647	0.677		
		R_Y		0.299	0.329	0.359		
	Green	G_x		0.247	0.277	0.307		
		G_Y		0.519	0.549	0.579		
	Blue	B_x		0.104	0.134	0.164		
		B_Y		0.093	0.123	0.152		
Viewing angle	Hor.	Θ_L	CR>10	60	70	—		(1)(4) Viewing Angle base on using EWV Polarizer , Reference Only
		Θ_R		60	70	—		
	Ver.	Θ_U		60	70	—		
		Θ_D		40	60	—		
Optima View Direction		12 o'clock						(5)

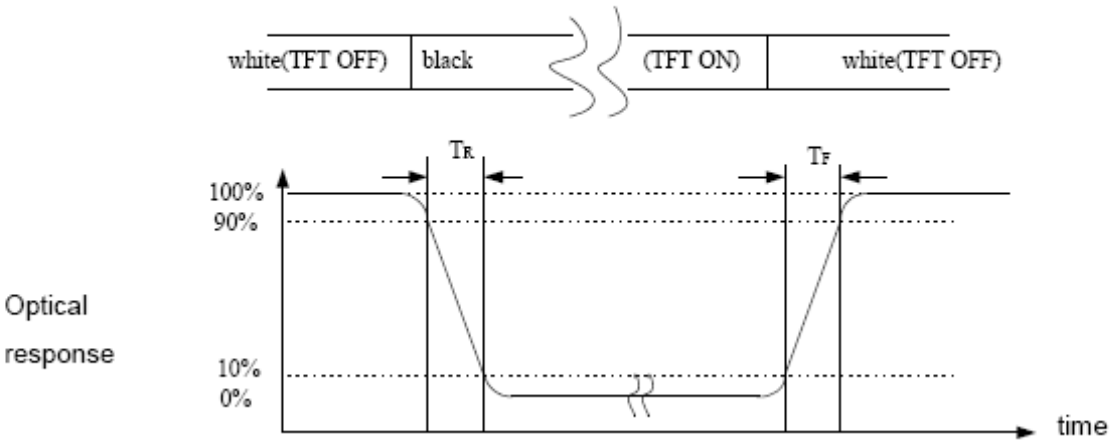
Note (1) Definition of Viewing Angle:



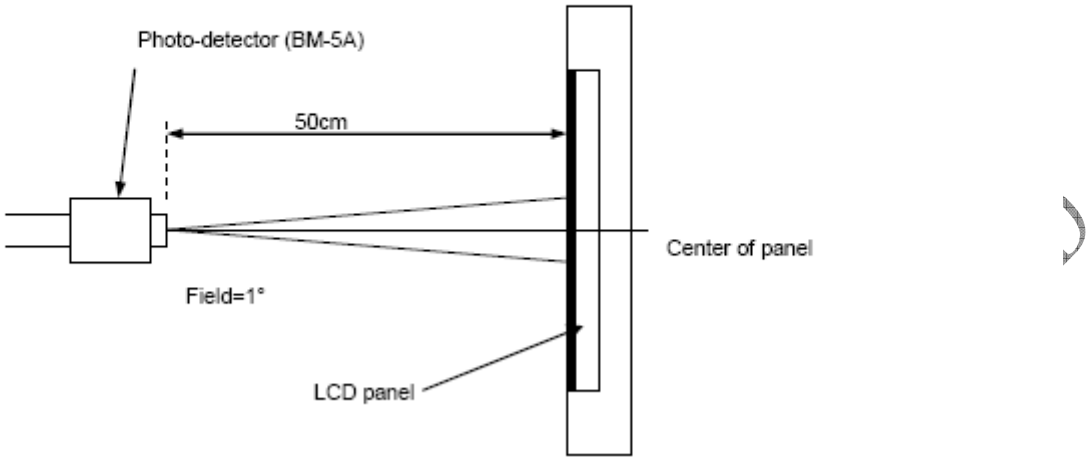
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

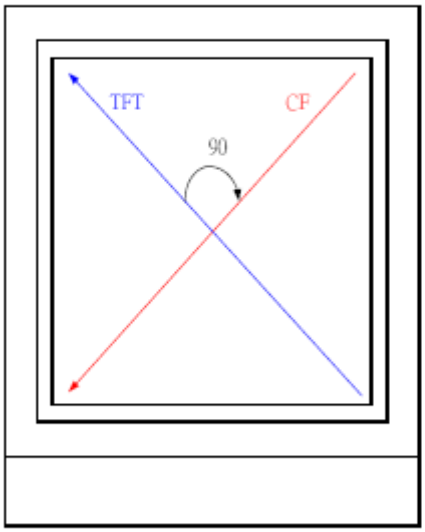
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



TFT Face up

10. Reliability Test Conditions And Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
①	High Temperature Storage	80℃±2℃×200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1,Air bublle in the LCD. 2,Sealleak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric Characteristics requirements shall be satisfied.
②	Low Temperature Storage	-30℃±2℃×200Hours	
③	High Temperature Operating	70℃±2℃×120Hours	
④	Low Temperature Operating	-20℃±2℃/120Hours	
⑤	Temperature Cycle(Storage)	-30℃±2℃ ⟺ 25℃ 80℃±2℃ (30min) (5min) (30min) 1cycle Total 10cycle	
⑥	Damp Proof Test	50℃±5℃×90%RH×120Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
⑨	ESD Test	Voltage: ± 8KV,R:330Ω,C:150PF,Air Mode,10times	

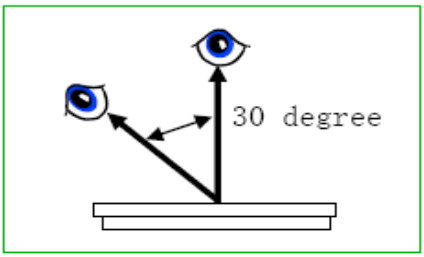
REMARK:
1,The Test samples should be applied to only one test item.
2,Sample side for each test item is 5~10pcs.
3,For Damp Proof Test,Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage,if it would be recovered to normal state after resetting,it would be judge as a good part.
5,EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11.Inspection Standard

This standard apply to TFT module specification.

1. Inspection condition:

Under daylight lamp 20~40W, product distance inspector'eye 30cm,incline degree 30° 。



2. Inspection standard

<table>
<tr><th>NO.</th><th>Item</th><th>Inspection standard</th><th>Rate</th></tr>
<tr><td>2.1</td><td>Dot</td><td>Case of Dot defect is below
① Bright Dot (whit spot) : “0”
② Dark Dot (black spot) : “0” (In case of Dark Dot on Main TFT LCD)
- NG if there's full Dot defect.
- Damaged less than the size of sub-pixel is not counted as defect
- Dots darker than the size of sub-pixel are not defined as bright dot defect

<table>
<tr><th>area
size （mm）</th><th>Acceptable number</th></tr>
<tr><td>Φ≤0.10</td><td>ignore</td></tr>
<tr><td>0.10＜Φ≤0.15</td><td>3</td></tr>
<tr><td>0.15＜Φ≤0.20</td><td>2</td></tr>
<tr><td>0.25＜Φ≤0.25</td><td>1</td></tr>
<tr><td>0.25＜Φ</td><td>0</td></tr>
</table></td><td rowspan="2">minor</td></tr>
<tr><td>2.2</td><td>line</td><td>
<table>
<tr><th colspan="2">Size （mm）</th><th>Acceptable number</th></tr>
<tr><td>ignore</td><td>W≤0.03</td><td>ignore</td></tr>
<tr><td>L≤4.0</td><td>0.03＜W≤0.04</td><td>2</td></tr>
<tr><td>L≤4.0</td><td>0.04＜W≤0.05</td><td>1</td></tr>
<tr><td></td><td>0.05＜W</td><td>Treat with dot non-conformance</td></tr>
</table></td></tr>
</table>

12. Handling Precautions

12.1 Mounting method

The LCD panel of FORMIKE ELECTRONIC CO,.LTD. module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent [recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Salfur (S)

If goods were sent without being sili8con coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Salfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 packing

- Module employ LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit. Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  It is recommended to store them as they have been contained in the inner container at the time of delivery from us

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

13. Precaution For Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to FORMIKE ELECTRONIC CO,.LTD,and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.