HF-BL200 BLE Module

User Manual

V1.0

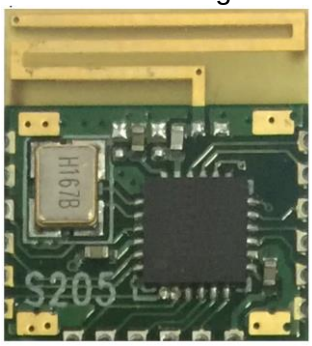
Key Features

- Bluetooth 4.2 (BLE) Communication
- Embedded BLE controller & host
  - GAP: broadcaster, observer & peripheral
  - “iCMD” command set to setup GAP, GATT, & other settings
- High power radio for long range
  - TX: up to +8 dBm
  - RX: -93 dBm sensitivity
  - Internal PCB Antenna or External Antenna Pin
- iCMD via SPI or UART interface
- Battery voltage: 1.9V~3.6V
- Current consumption:
  - 3.5~17.5uA sleep modes
  - ~28mA RF active
- Average current:
  - 20mS/0.5S/4S ADV: 3500/140/22uA
  - 30mS/100mS/4S CONN: 1000/320/11uA
- Package:
  - (12.75 x 12 x 2)mm (Internal)
  - (9 x 12 x 2)mm (External)
- Bluetooth SIG QDID: 91979,
- Declaration ID D033798

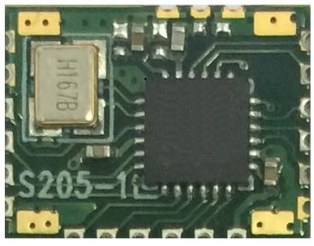
Applications

Add to existing MCU solutions for BLE connectivity:

- Toys: remote control cars, planes and quadcopters
- Lighting & home automation
- Remote controls
- Power-management



HF-BL200-1



HF-BL200-0

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1 INTRODUCTION

HF-BL200 is a Bluetooth Low Energy (BLE) integrated circuit designed to provide BLE connectivity to MCU and hosted systems. It consists a fully integrated 2.4GHz radio transceiver, modem, and baseband processor for Bluetooth Smart®. Once set up, HF-BL200 runs autonomously, automatically running advertising events, scanning, and maintains connection with minimal host effort; pin **INT0** is used to notify host intervention, and pin **INT1** may be used by host to prevent HF-BL200 entering sleeping states (e.g. when setting up database, or testing purposes).

An integrated baseband processor on HF-BL200 handles the BLE controller and protocol host functions. The system host needs to set up the contents of the BLE database, as well as the connection settings of HF-BL200. An "iCMD" command set is developed for HF-BL200 setup, including GAP, GATT and connection parameters. SPI & UART interface are supported, selected by strapping. Patches are also supported via the iCMD interface. Typical NV memory usage on the system host for the HF-BL200 setup is 4kB to 8kB, depending on the complexity of the databases, and whether patches are needed/supported.

The HF-BL200 radio is designed with low BOM count and long-range in mind. RF I/O is single pin, and no matching is required for typical applications (0 dBm). The radio can provide up to +10 dBm output power for long-range applications such as toys, lighting, or home automation.

The HF-BL200 is compliant with the Bluetooth 4.0 standard. 4.2 hardware features are included on chip, and will be enabled in subsequent releases.

1.1 FEATURES

Radio

- 2.4GHz Bluetooth Low Energy (BLE) transceiver
- Single RF pin, no RF matching for typical power levels
- TX: up to +8 dBm output power (0~3 dBm typical)
- RX: -93 dBm sensitivity
- Integrated RSSI

Power Management

- Three low-power modes: dormant, hibernate, and sleep
  - Hibernate: 3.5uA typ., internal RC32k
  - Sleep: 17.5uA typ., RF XTAL core active
- Active: processor running and can accept iCMD commands
  - RF activities: TX, RX, automatic calibration every packet/event
  - Link layer processing
  - Host processing
  - Set to low-power modes based on host setup and current protocol state

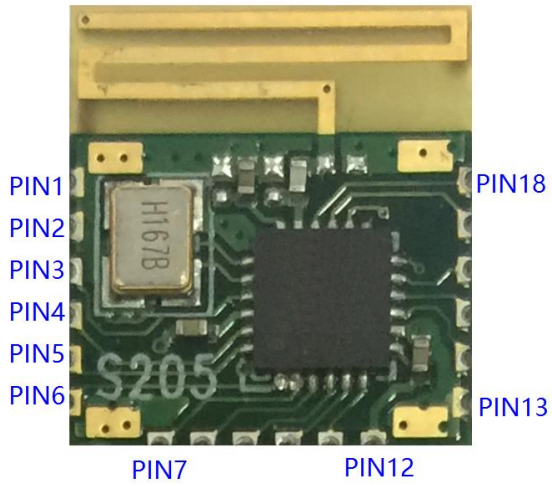
Bluetooth Smart®

- Bluetooth 4.2 Low Energy
- Integrated & autonomous link layer engine, BLE security support
- GAP roles supported: broadcaster, observer, & peripheral
- GATT features: GATT server; up to 22 bytes for each characteristic, expandable to 512 bytes; up to 38 characteristics
- Multi-role: Scan while advertising, scan while connected, and advertising while connection supported

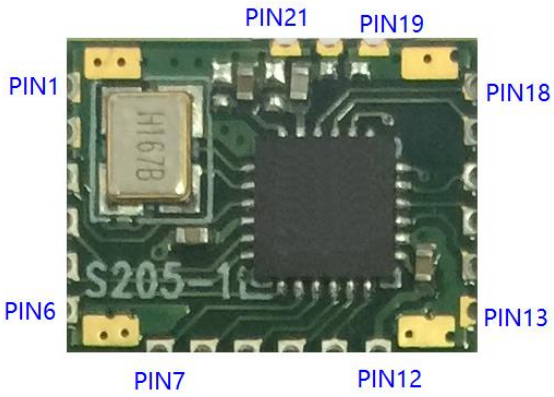
Digital Interfaces

- iCMD: SPI or UART, selectable by boot strapping
- **INT0**: HF-BL200 interrupt to host
- **INT1**: HF-BL200 “wake-lock”, set high to prevent HF-BL200 entering sleep states
- **UART_DTM**: UART interface for DTM tests
- **UART_DEB**: UART for protocol debugging

2 PIN INFORMATION



HF-BL200-1 Pin Definition



HF-BL200-0 Pin Definition

Pin #	Name	Function	Description
1,2,13 19,21	**GND**	Power	Power Ground.
3	**VDDQ**	Power	e-fuse power pin **VDDQ** is used during e-fuse programming, leave open or tie to ground in normal use. See E-Fuse section for more details
4	**INT1**	DIG I	Interrupt input to HF-BL200 (wake lock), set high to prevent HF-BL200 entering sleep states P23
5	**INT0**	DIGO	Interrupt to external MCU, active-low P24

6~9	**CMIF0(pin6)** **CMIF1** **CMIF2** **CMIF3(pin9)**	DIG I/O	iCMD interface, set to SPI or UART by strapping CMIF2 P01~P04
10~11	NC	NC	No connection
12	**VBATT**	Power	Power, 1.9V~3.6V
14	**UART_DTM_TX**	DIG I/O	UART interface for DTM tests UART_TX P09
15	**UART_DTM_RX**	DIG I/O	UART interface for DTM tests UART_RX P10
16	**HW_RSTN**	DIG I	Hardware reset pin (active low)
17	**UART_DEB_TX**	DIG I/O	Debugging UART_TX interface (protocol debug) P15
18	**UART_DEB_RX**	DIG I/O	Debugging UART_RX interface (protocol debug) P16
21	**RF**	RF	RF Antenna pin

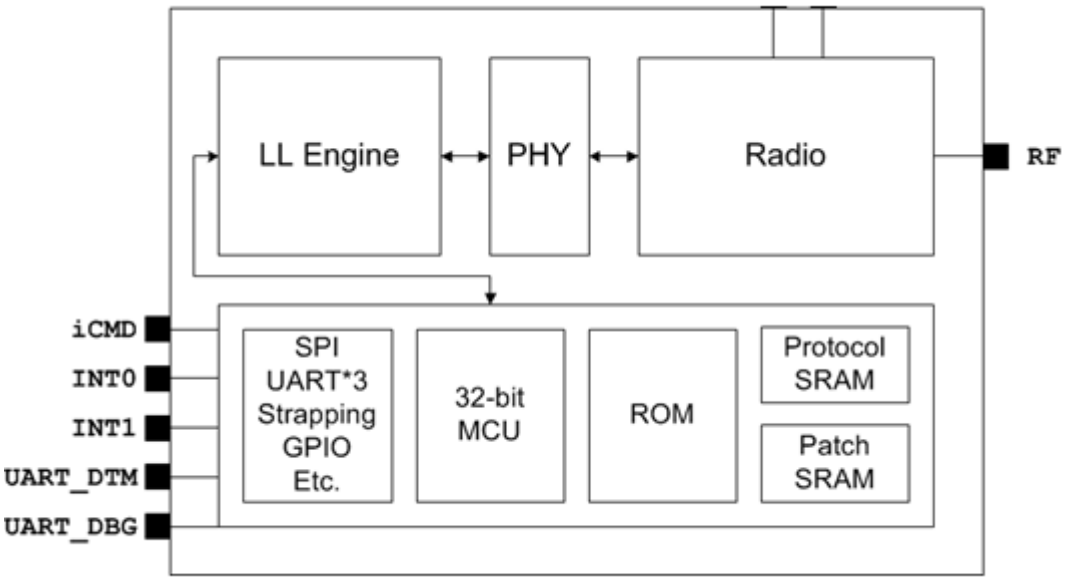
Note 1: the digital I/O pins **UART_TX**, **UART_RX**, **UART_DEB_TX**, **UART_DEB_RX** are unused in normal functions, leave open. Connecting to logic high or low may result in malfunction.

Note 2: **VDDQ** is used during e-fuse programming, leave open or tie to ground in normal use. See E-Fuse section for more details.

Note 3: pin 10 and pin 11 are reserved for manufacturing tests only. Leave open. Connecting pin 10 and 11 to any voltages (VBATT or GND) may result in extra leakage current and unexpected behavior during normal operation.

3 SYSTEM OVERVIEW

HF-BL200 consists of a 2.4GHz RF transceiver, PHY (modem) and packet assembler/disassembler, hardware link-layer engine, and an internal MCU running BLE protocol on ROM. HF-BL200 communicates with the host system via **CMIF0~3** pins, either UART or SPI interface, configurable by strapping. **INT0** output pin is used to notify host system to intervene, and **INT1** input pin is used as wake-lock to keep HF-BL200 from entering sleep states.



3.1 POWER STATES

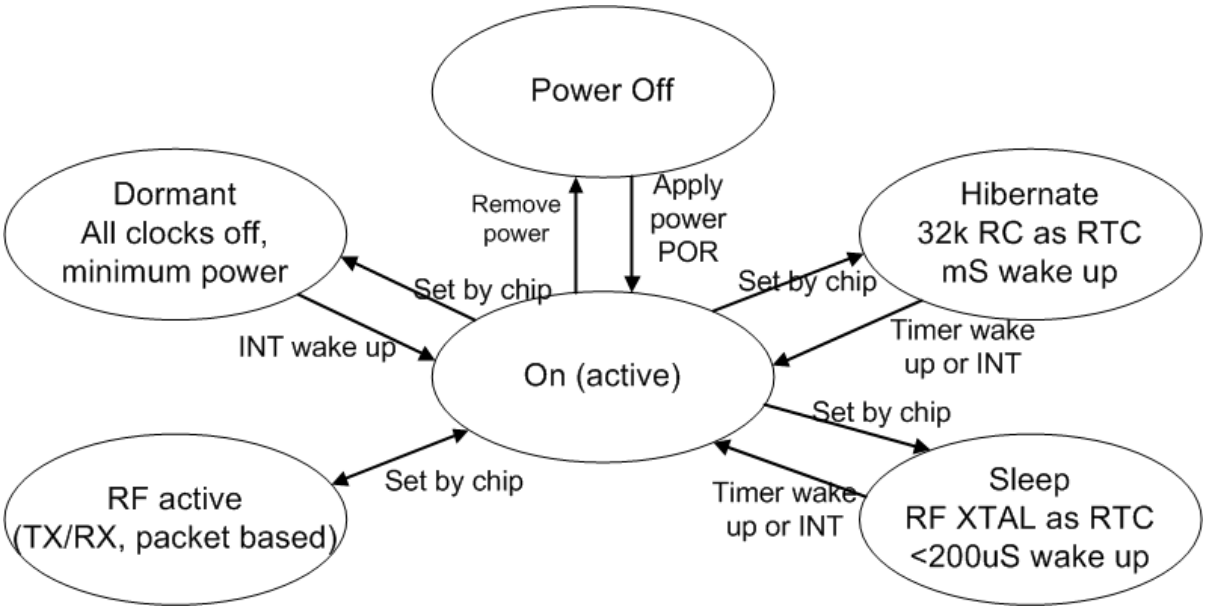
HF-BL200 consists of 4 power states: dormant, hibernate, sleep and active. The different power states have different level of current consumption and activities.

Dormant: all chip activities are halted. This state is currently disabled.

Hibernate: 32k RC as RTC

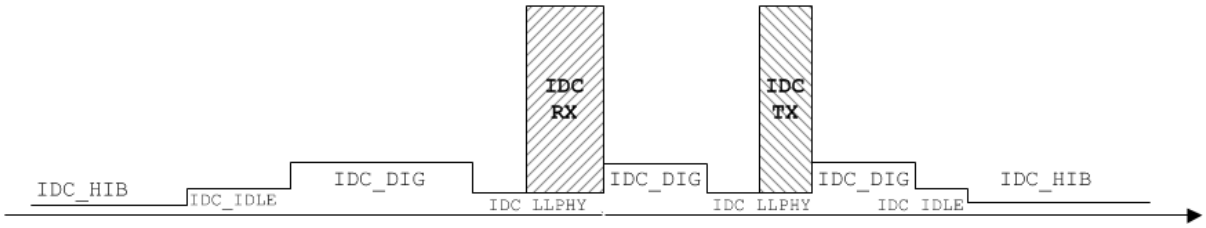
Sleep: 32k RC as RTC , XTAL core running at low current for faster startup.

Active: system on, set up protocol parameters and databases, running BLE protocol and RF activities. The 32k RC clock is calibrated with the RF crystal during active state, ensuring frequency accuracy up to ±250ppm during hibernate state.



Once set up, the HF-BL200 power management algorithm will enter low-power states when possible, and wake up for advertising, connection and calibration activities as needed.

A current profile of a typical BLE transaction:



3.2 RADIO

The HF-BL200 architecture consists of a direct frequency modulation (DFM) transmitter and a low-IF receiver. The synthesizer is calibrated before every TX/RX event to ensure frequency accuracy and modulation quality at all times, over all temperature and voltage range.

The default RF crystal frequency is 16MHz. To comply with BLE specifications, the ppm requirement is ±40ppm or smaller. HF-BL200 can support other crystal frequencies: 12MHz, 24MHz, 26MHz, 32MHz and 40MHz. Support for other crystal frequencies require e-fuse programming.

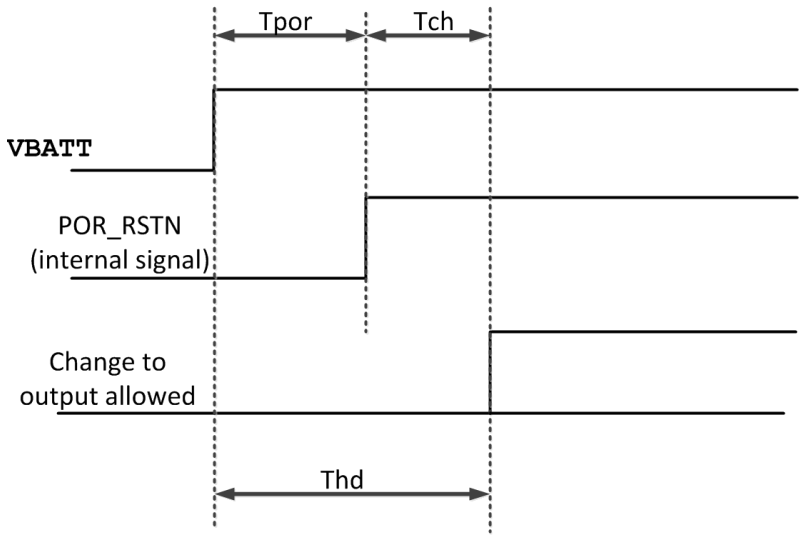
HF-BL200 has on-chip CLOAD for RF crystal, supporting crystal of 9pF CLOAD (differential) by default. The CLOAD is tunable, up to 10pF, and can be set by e-fuse programming.

3.3 BOOT STRAPPING

HF-BL200 iCMD interface supports UART and SPI interfaces. The choice is set by boot-strapping pin **CMIF2** during POR. The interface-mapping table for SPI or UART interface is shown below.

Pin Name	SPI definition	UART definition	Notes
CMIF0	**SCLK**	**NCTS**	Not used for UART
CMIF1	**CSN**	**RXD**	
CMIF2	**MISO**	**TXD**	Strapping pin, pull high for SPI, leave open for UART
CMIF3	**MOSI**	**NRTS**	Not used for UART

The timing diagram and specifications for strapping pin is shown below:



Parameter	Description	Min.	Typ.	Max.	Unit
Tpor	Time from power ready to POR signal	2			mS
Tch	Time from POR signal to strap latched	1			mS
Thd	Thd = Tpor + Tch	3			mS

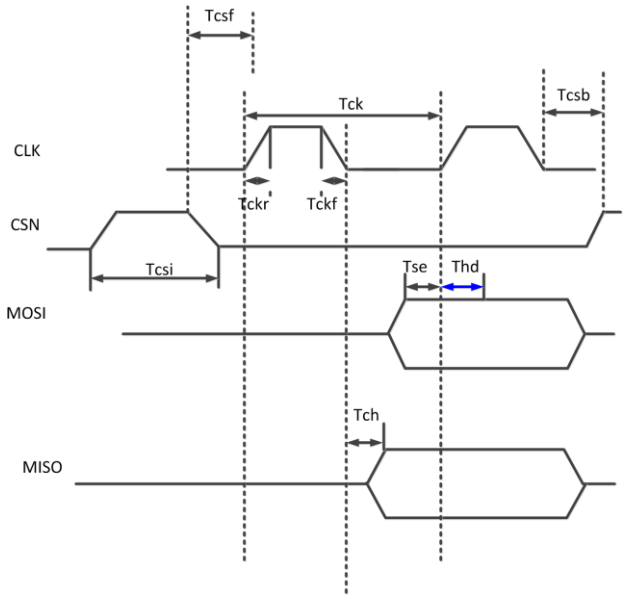
3.4 iCMD INTERFACE

HF-BL200 is programmed through the **CMIF0~4** pins using iCMD interface. Depending on strapping option **CMIF** may be set to SPI or UART interface for communication with host device. In addition to the 4 **CMIF** pins, **INT0** and **INT1** are used for HF-BL200-to-host and host-to-HF-BL200 notifications. The signal **INT0** interrupt is an active high signal, and a tie-low resistor is recommended. HF-BL200 may malfunction if this pin is improperly tied to high during POR.

Details of the iCMD command set, setup in SPI/UART mode, API, and sample codes are described in accompanying application notes.

The baud rate for iCMD operating in UART mode is 9600. The maximum clock speed for iCMD operating in SPI mode is 3MHz.

Timing diagram and specifications for iCMD operating in SPI mode is shown below:



Parameter	Description	Min.	Typ.	Max.	Unit
Tcsf	CSN to CLK positive edge	1000			nS
Tcsb	CLK negative edge to CSN time	1000			nS
Tcsi	Width between two CSN	1000			nS
Tck	CLK time	333			nS
Tckr	CLK rise time			TBD	nS
Tckf	CLK fall time			TBD	nS
Tse	MOSI data input setup time	5			nS
Thd	MOSI data input hold time	5			nS
Tch	MISO data output change time	15			nS

3.5 UART_DTM, UART_DEB & DEBUGGING INTERFACES

UART_DTM pins are used for SIG DTM tests. A special iCMD command enables the UART function for DTM test; system host should have a test-mode procedure to set HF-BL200 to DTM mode. Test pins or probe pads to **UART_DTM** should be provided in final product for DTM tests.

UART_DEB pins provide debugging log for the BLE protocol. Leave the pins open; tying the pins to logic 0 or 1 will cause malfunction to module. Test pins or probe pads to **UART_DEB_TX** and **UART_DEB_RX** are recommended during engineering phase and final product for BLE protocol debugging.

3.6 E-FUSE

A 256-bit e-fuse on HF-BL200 is used to store fixed hardware settings. E-fuse settings include:

1. MAC address
2. Crystal CLOAD setting
3. Crystal frequency
4. PMU settings

Preset values are on-chip, so HF-BL200 is functional without e-fuse programming.

4 ABSOLUTE MAXIMUM RATINGS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
VPIN	Limiting voltage on pin		-0.1		VBATT	V
TSTORE	Storage temperature	TBD	-50		150	°C
T_VRISE	Power supply rise time	TBD	5		100	mS
VBATT_L	Supply voltage limit		-0.1		3.6	V
ESD_HBM	ESD, human body model	1			4000	V
ESD_MM	ESD, machine model	1			100	V
ESD_CDM	ESD, charged device model	1			500	V

Note 1: test chips preliminary results

5 OPERATING CONDITIONS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
VBATT	Battery supply voltage		1.9		3.6	V
VPP	E-fuse programming voltage		2.4	2.5	2.6	V
VIO	I/O voltage		0		VBATT	V
T	Temperature		-40		+85	°C

Note 1: PIN7 & PIN18 connect together on board to same VBATT voltage.

Note 2: **VDD** pin is for decoupling cap only; applying voltage to it or using it for external voltage supply may cause malfunction or damage to chip.

6 ELECTRICAL SPECIFICATIONS

6.1 16MHZ CRYSTAL

Parameter	Description	Note	Min.	Typ.	Max.	Unit
F_16MXTAL	Crystal Frequency			16.0		MHz
F_16MTOL	Frequency tolerance				±40	ppm
RS				TBD		
PD				TBD		
CL	Differential C load, default			9		pF
I_16MXTAL	Core dc current, on			25		uA
IS_16MXTAL	Core dc current, sleep			7		uA
T_16MXTAL	Startup time, 16M XTAL			200		uS

6.2 32KHZ RC OSCILLATOR

Parameter	Description	Note	Min.	Typ.	Max.	Unit
F_32KRC	Frequency (nominal)			32787		Hz
F_32KRCTOL	Frequency tolerance				±250	ppm
I_32KRC	dc current			800		nA
T_32KRC	Startup time			0.2		mS

6.3 POWER MANAGEMENT

Parameter	Description	Note	Min.	Typ.	Max.	Unit
I_DORM	Dormant state current			2.5		uA
I_HIB	Hibernate state current			3.5		uA
I_SLEEP	Sleep state current			17.5		uA
I_ON	On state current, idle			7.5		mA
I_TX0DBM	TX mode, 0 dBm			27.7		mA
I_TX10DBM	TX mode, +10 dBm			47.1		mA
I_TXN20DBM	TX mode, -20 dBm			14.2		mA
I_RX	RX mode			26.8		mA

Note: Dormant state is a reserved state and equivalent to power-down.

6.4 RADIO SPECIFICATIONS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
FRF_RANGE	Operating frequency range		2400		2483	MHz
FD_BLE	Frequency deviation, BLE		225	250	275	kHz

6.5 TX SPECIFICATIONS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
PRF_MAX	Maximum output power			8		dBm
PRF_TYP	Typical output power			2		dBm
PRF_RANGE	Output power range			30		dB
PRF_LP	Quiet mode output power			-40		dBm
PRF_BLE_2M	Spurious @ 2MHz offset				-54	dBc
PRF_BLE_3M	Spurious @ 3MHz offset				-58	dBc

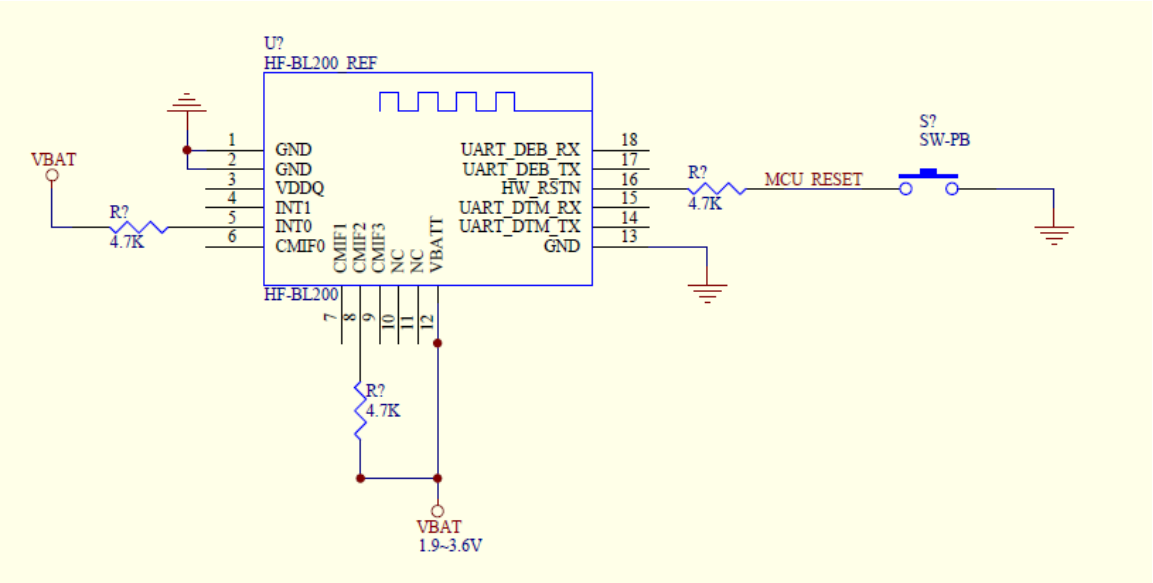
6.6 RX SPECIFICATIONS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
PRX_MAX	Maximum received power			2		dBm
PRX_MIN_IDEAL	Minimum received power, ideal			-93.5		dBm
PRX_MIN_DIRTY	Minimum received power, dirty			-92		dBm
CI_CO				7		dB
CI_1ST				1		dB
CI_2ND				-28		dB
CI_3+N				-38		dB
CI_IMG				-21		dB
CI_IMG1				-23		dB
P_IMD				-38	-35	dBm

6.7 RSSI SPECIFICATIONS

Parameter	Description	Note	Min.	Typ.	Max.	Unit
RSSI_RNG	RSSI Range			45		dB
RSSI_PMIN	RSSI minimum level			-83		dBm
RSSI_STEP	RSSI step size			0.4		dB
RSSI_ACC	Accuracy of RSSI		-5		+5	dB

7 APPLICATION EXAMPLE: SPI INTERFACE TO HOST



- **CMIF2**: resistor tie-high for SPI iCMD interface; leave open for UART
- **UART_DTM:** leave open, reserve test pads/pins for DTM tests.
- **HW_RSTN**: an external switch is shown in example, can be connected to host to reset module. Module need to be set up by host after hardware reset.
- **UART_DEB**: leave open, reserve test pad/pins for protocol debugging.
- **VDDQ**: leave open.
- **INT0**: active-low interrupt pin, resistor tie to VBAT
- **INT1**: Interrupt input to HF-BL200 (wake lock), set high to prevent HF-BL200 entering sleep states
- VBATT: Connect to VCC input(1.9~3.6V).

8 ORDER INFORMATION